CURRICULUM AND SYLLABUS

FOR

M. TECH.

IN

VLSI & EMBEDDED SYSTEMS

(With Effect from Academic Year 2024 - 25)

DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY SURAT
GUJARAT - 395007

SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY SURAT

VISION

To be one of the leading Technical Institutes disseminating globally acceptable education, effective industrial training and relevant research output.

MISSION

To be a globally accepted centre of excellence in technical education catalyzing absorption, innovation, diffusion and transfer of high technologies resulting in enhanced quality for all the stakeholders.

DEPARTMENT OF ELECTRONICS ENGINEERING

MISSION

The mission of the Department of Electronics Engineering is to contribute to society and industry through excellence in education, research, innovations, and ethics by stakeholders.

VISION

The vision of the Department of Electronics Engineering is to aim to achieve quality in education and research to create leading Electronics engineers, researchers, and entrepreneurs.

DEPARTMENT OF ELECTRONICS ENGINEERING

SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY SURAT

GUJARAT - 395 007

M. Tech. Programme (VLSI & Embedded Systems)

Programme Educational Objectives (PEOs):

Sr. No.	PEO Description
PEO-1	To prepare quality Postgraduates in Electronics Engineering with specialization in VLSI and Embedded System design with in-depth knowledge of relevant subjects.
PEO-2	To create professionals who can formulate, analyze, synthesize and be able to pursue higher research for engineering problems.
PEO-3	To develop skilful manpower in the area of VLSI and Embedded Systems who can design and manufacture state-of-the art systems/products to meet the requirements of industry.
PEO-4	To disseminate skills and experiences to the society by becoming an entrepreneur or leader.

Programme Outcomes (POs):

Sr. No.	PO Statement
PO-1.	Postgraduates will be able to identify research gaps through literature survey, apply appropriate research methodologies to propose solutions, conduct experiments and validate results through realistic scenarios and constraints.
PO-2.	Postgraduates will be able to communicate effectively in both oral and written context in the form of technical papers, thesis reports, design documents and seminar presentations.
PO-3.	Postgraduates will be able to demonstrate expertise in VLSI and Embedded System Design by prototype/product development.
PO-4.	Postgraduates will apply knowledge acquired in Mathematics, Science and Engineering to solve VLSI and Embedded System Design problems.
PO-5.	Postgraduates will be able to analyze complex engineering problems critically, apply reasoning for synthesis to make creative advances for conducting research.
PO-6.	Postgraduates will learn and use the latest hardware and software tools/platforms, modern techniques and technologies, optimization methods to solve complex engineering problems.

Course Structure and Scheme of Evaluation (Semester wise)

M. Tech. I (EC), I Semester (VLSI & Embedded Systems)											
Sr. No.	**Course Name**	**Code**	**Teaching Scheme**			**Credit**	**Examination Scheme (Marks)**			**Total**	**Notional hours of Learning (Approx.)**
			L	**T**	**P**		**Theory**	**Tutorial**	**Practical**		
1	Digital VLSI Design	ECVL101	3	0	0	3	100	--	--	100	55
2	MOS Devices & Technology	ECVL103	3	0	0	3	100	--	--	100	55
3	Embedded Systems	ECVL105	3	0	0	3	100	--	--	100	55
4	Elective – I	ECVL1XX	3	0	0	3	100	--	--	100	55
5	Elective – II	ECVL1XX	3	0	0	3	100	--	--	100	55
6	VLSI LAB – I	ECVL107	0	0	6	3	--	--	150	150	100
7	Seminar	ECVL109	0	0	4	2	--	--	100	100	70
Total			**15**	**0**	**10**	**20**	**500**	**--**	**250**	**750**	**445**
Total Contact Hours per week: **25**											

M. Tech. I (EC), II Semester (VLSI & Embedded Systems)											
Sr. No.	**Course Name**	**Code**	**Teaching Scheme**			**Credit**	**Examination Scheme (Marks)**			**Total**	**Notional hours of Learning (Approx.)**
			L	**T**	**P**		**Theory**	**Tutorial**	**Practical**		
1	Analog VLSI Design	ECVL102	3	0	0	3	100	--	--	100	55
2	Real-Time Systems	ECVL104	3	0	0	3	100	--	--	100	55
3	Institute Elective – III	ECVL1XX	3	0	0	3	100	--	--	100	55
4	Elective – IV	ECVL1XX	3	0	0	3	100	--	--	100	55
5	Elective – V	ECVL1XX	3	0	0	3	100	--	--	100	55
6	VLSI LAB - II	ECVL106	0	0	6	3	--	--	150	150	100
7	Mini Project	ECVL108	0	0	4	2	--	--	100	100	70
Total			**15**	**0**	**10**	**20**	**500**	**--**	**250**	**750**	**445**
Total Contact Hours per week: **25**											

M. Tech. II (EC), III Semester (VLSI & Embedded Systems)											
Sr. No.	**Course Name**	**Code**	**Teaching Scheme**			**Credit**	**Examination Scheme (Marks)**			**Total**	**Notional hours of Learning (Approx.)**
			L	**T**	**P**		**Theory**	**Tutorial**	**Practical**		
1	Dissertation – Phase I	ECVL201	0	0	28	14	-	-	350	350	560
2	MOOC – I*	φ	-	-	-	3/4	100	-	-	100	70/80
3	MOOC – II*	φ	-	-	-	3/4	100	-	-	100	70/80
Total			**0**	**0**	**28**	**20/21/22**	**200**	**0**	**350**	**550**	**700/720**
Total Contact Hours per week: **28 + NPTEL (Course Hours) × 2**											

***** NPTEL, SWAYAM and other Massive Open Online Course (MOOC) approved by DAAC

φ As per 66th IAAC, Dated 20th March, 2024, Resolution No. 66.34 and 61st Senate resolution No. 4, 25th April, 2024

M. Tech. II (EC), IV Semester (VLSI & Embedded Systems)											
Sr. No.	**Course Name**	**Code**	**Teaching Scheme**			**Credit**	**Examination Scheme (Marks)**			**Total**	**Notional hours of Learning (Approx.)**
			L	**T**	**P**		**Theory**	**Tutorial**	**Practical**		
1	Dissertation – Phase II	ECVL202	0	0	40	20	-	-	600	600	800
Total			**0**	**0**	**40**	**20**	**-**	**-**	**600**	**600**	**800**
Total Contact Hours per week: **40**											

LIST OF SUBJECTS FOR ELECTIVE I & II (Semester – I):		
1.	Semiconductor IC Technology	ECVL111
2.	Hardware Description Language	ECVL113
3.	Processor Architecture	ECVL115
4.	Testing and Verification of VLSI Circuits	ECVL117
5.	Nanoelectronics	ECVL119
6.	Advanced Material Characterization Techniques	ECVL121
7.	Advance DSP	ECCS105
8.	Information Theory & Coding	ECCS111
9.	Machine Learning and Applications	ECCS121

LIST OF SUBJECTS FOR INSTITUTE ELECTIVE - III (Semester – II):		
1.	Solar Photovoltaic Technology	ECVL170
2.	MEMS	ECVL172
3.	Foundations of VLSI CAD	ECVL174
4.	Semiconductor Device Modelling	ECVL176
5.	Fundamentals of Semiconductor Package Manufacturing and Test	ECVL178

LIST OF SUBJECTS FOR ELECTIVE IV & V (Semester – II)		
1.	Low Power VLSI Design	ECVL112
2.	VLSI Architectures for DSP	ECVL114
3.	VLSI System Design	ECVL116
4.	SOC Design	ECVL118
5.	CMOS RF IC Design	ECVL120
6.	Nanoscale Devices	ECVL122
7.	Semiconductor Packaging	ECVL124
8.	Neuromorphic Computing	ECVL126
9.	Mixed Signal IC Design	ECVL128
10.	Memory Technology	ECVL130
11.	High-Speed Interconnect	ECVL132
12.	Image Processing & Computer Vision	ECCS102
13.	Wireless Communication	ECCS104
14.	Microwave Integrated Circuits	ECCS116
15.	Speech Processing and Applications	ECCS130

M. Tech. I (VLSI & Embedded Systems) Semester – I DIGITAL VLSI DESIGN ECVL101	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand VLSI design flow and CMOS inverter
CO2	Implement CMOS combinational and Sequential logic
CO3	Analyze circuit characteristic
CO4	Evaluate circuit performance
CO5	Design digital subsystems

2. Syllabus

INTRODUCTION TO VLSI DESIGN (04 Hours)

Historical Perspective, Design Hierarchy, Concepts Of Regularity, Modularity And Locality, VLSI Design Challenges, Introduction of VLSI Design Flow:, From Custom to Semi Custom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology: Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow; Array-Based Implementation Approaches: Pre-Diffused (or Mask-Programmable) Arrays, Pre-Wired Arrays.

CMOS INVERTER BASICS and COMBINATIONAL LOGIC CIRCUIT (09 Hours)

Brief introduction to MOS transistor models and SPICE parameters; process parameters and design rules

Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter (The Static Behavior): Switching Threshold, Noise Margins, Robustness Revisited; Performance of CMOS Inverter (The Dynamic Behavior): Computing the Capacitances, Propagation; Delay: First-Order Analysis, Propagation Delay from a Design Perspective; Power, Energy and Energy- Delay: Dynamic Power Consumption, Static Consumption, Perspective: Technology Scaling and its Impact on the Inverter Metrics

CMOS Combinational Logic Circuits, Complex Logic Circuits, Layout Techniques, Behavior Of MOS Logic Elements, CMOS Pass Gate and Transmission Gate, Design of combinational circuit using pseudo-nMOS and DCVSL and DSL logic gates. CPL, DPTL and swing restored pass transistor logic styles

SEQUENTIAL LOGIC CIRCUIT (08 Hours)

Timing Metrics for Sequential Circuits, Classification of Memory Elements; Static Latches and Registers: The Bistability Principle, Multiplexer-Based Latches, Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops—Writing Data by Pure Force; Dynamic Latches and Registers: Dynamic Transmission-Gate Edge-triggered Registers, C2MOS—A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR); Alternative Register Styles: Pulse Registers, Sense-Amplifier Based Registers; Pipelining (An approach to optimize sequential circuits): Latch- vs. Register-Based Pipelines, NORA-CMOS—A Logic Style for Pipelined Structures; Non-Bistable Sequential Circuits: The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits; Perspective: Choosing a Clocking Strategy

DYNAMIC LOGIC CIRCUIT **(05 Hours)**

Dynamic Logic (Basic Principles), Speed and Power Dissipation of Dynamic Logic, logic styles including np, Domino, NORA and TSPC logic, Issues in Dynamic logic due to charge sharing and race conditions, Cascading Dynamic Gates; Perspectives: How to Choose a Logic Style

CIRCUIT CHARACTERIZATION, PERFORMANCE ESTIMATION AND TESTING **(06 Hours)**

Interconnect, Estimation of Interconnect Parasitic, Delay Estimation, Logical Efforts And Transistor Sizing, Power Dissipation, Design Margin, Reliability, Testing: Introduction, Automatic Test pattern Generation (ATPG), Design for Test (DFT), Buit-in self Test (BIST)

DIGITAL SUBSYSTEM DESIGN **(13 Hours)**

Design of IO buffers and on chip load drivers; PLL, clock generation and clock buffering; design of memory cells and sense amplifiers

Design of adders - Ripple carry, Manchester carry, carry look ahead, carry select and carry save

Design of multipliers (for unsigned and signed) - sequential, parallel, carry save, Booth multipliers; Wallace tree structures

Design of shifters and floating point arithmetic units

Total Contact Time: = 45 Hours

3. Books Recommended

1. Rabaey Jan M., Chandrakasan Anantha and Borivoje Nikolic, "Digital Integrated Circuits (Design Perspective)", 2nd Ed., Prentice Hall of India, 2016 (Reprint).
2. Kang and Leblebici,“CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, 4th Edition, 2019
3. Baker R. Jacob, Li H. W. & Boyce D. E.,“CMOS Circuit Design, Layout And Simulation”, Wiley, 4th Edition, 2009
4. Weste and Harris,“CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson Education, 4th Edition, 2020
5. Pucknell and Eshraghian: “Basic VLSI Design”, Prentice Hall of India, 3rd Edition, 2003

M. Tech. I (VLSI & Embedded Systems) Semester – I MOS DEVICES AND TECHNOLOGY ECVL103	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understanding and analysis of semiconductor Physics and PN Junction
CO2	Understanding of MOS capacitor and MOSFET
CO3	Derivation of I-V and C-V of MOSFET and MOS Capacitor respectively
CO4	Evaluation of advanced electronic devices
CO5	Design of MOSFET and MOS Capacitor

2. Syllabus

PHYSICS OF SEMICONDUCTOR AND PN JUNCTION (15 Hours)

Allowed and Forbidden Bands, Band Structure, Density of States Function, Statistical Mechanics, Electrical Conduction Semiconductor In Equilibrium, Carrier Transport Phenomena, Non-Equilibrium Excess Carries in Semiconductor, PN Junction Current, Small Signal Model, Generation And Recombination Current, Junction Break Down

MOS CAPACITOR and MOSFET (15 Hours)

Metal Semiconductor and Hetero Junctions, Two Terminal MOS Structure, CV Characteristics, MOSFET Operation, I-V derivation, Frequency Limitation, Short channel effects, MOSFET scaling, Radiation, and hot electron effect

LARGE SIGNAL AND LOW-FREQUENCY SMALL SIGNAL MODELING (10 Hours)

Quasi-Static modeling and Non quasi static modeling of MOSFET, Transit time, Equivalent model of MOSFET with extrinsic resistance and capacitance, low frequency small signal modeling for weak, moderate and strong region of operation.

ADVANCE MOS DEVICES (05 Hours)

Introduction of advanced devices FDSOI, FinFET, Tunnel FET, Nanosheet device, HEMT

Total Contact Time: = 45 Hours

3. Books Recommended

1. Donald Neaman, “Semiconductor Physics and Devices”, McGraw Hill, 4th Edition, 2012
2. S. M. Sze, “Semiconductor Devices, Physics And Technology”, John Wiley and Son s 3rd Edition, 2007
3. S. M. Sze, “Physics of Semiconductor Devices”, John Willey 3rd Edition, 2007
4. B. G. Streetman,“Solid State Electronics Device”, HI, 2005
5. Y. Tsividis, Colin McAndrew, “Operation And Modeling Of The MOS Transistor”, Oxford university press, 3rd Edition, 2012
6. Y. Taur and H. Ning, “Fundamentals of Modern VLSI Devices” Cambridge University Press, 2021.
7. M. S. Lundstrom and J. Guo, “Nanoscale Transistors: Device Physics, Modeling and Simulation” Springer, 2006
8. D. Esseni, P. Palestri, and L. Selmi, “Nanoscale MOS Transistors: Semi-Classical Transport and Applications”, Cambridge University Press, 2011.

Additional Resources:

1. M. Alam, "ECE 695A Reliability Physics of Nanotransistors," https://nanohub.org/resources/16560.
2. M. Lundstrom, "ECE 612: Nanoscale Transistors (Fall 2008)," https://nanohub.org/resources/5328.
3. Mark Lundstrom (2008), "Physics of Nanoscale MOSFETs," https://nanohub.org/resources/5306.

Relevant Journals and Conference papers.

M. Tech. I (VLSI & Embedded Systems) Semester – I EMBEDDED SYSTEMS ECVL105	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand Embedded systems and describe CPU architectures and variety of microcontrollers
CO2	Demonstrates CPU processor, its modes, exception handling, instruction pipelining and basic programming
CO3	Implementation with Assembly and C language programming for ARM Cortex-M.
CO4	Analyze 32-bit ARM microcontroller architecture, External Memory, Counters & Timers, Serial Data Input/Output and Interrupts. Design for interfacing Keys, LED/LCD Displays, ADC and DAC.
CO5	Design a typical cost-effective real-world embedded system with appropriate hardware/software components and embedded OS

2. Syllabus

INTRODUCTION TO EMBEDDED SYSTEMS **(08 Hours)**

Overview and Characteristics of Embedded Systems, Classification and Application Areas, Process of Embedded System Development, RISC Vs CISC CPU Architectures, 8/16/32 bit Microcontrollers Family, Components in embedded system development environment (IDE)

ARM CORTEX M3/M4 ARCHITECTURE **(10 Hours)**

Overview of ARM Cortex family, Operation modes and states, Registers, Special Registers, Floating point Registers, Memory system and MPU, Exception and interrupts, System control block, OS Support features, ARM Instruction Set Architecture, Arithmetic and Logic, Load and Store, Branch and Conditional Execution

PROGRAMMING CORTEX M3/M4 IN ASSEMBLY and C **(10 Hours)**

Structured Programming, Subroutines, 64-bit Data Processing, Mixing C and Assembly, Interrupt and NVIC, Fixed-point and Floating-point Arithmetic, Writing optimized ARM assembly/C code, Exception and fault handling routines

USING EMBEDDED OS **(08 Hours)**

Introduction to Embedded OS, Task and Threads, Creation of Threads, Inter-thread communications, Signal event, Semaphores, Message queue, OS based programming examples.

PERIPHERAL INTERFACING **(09 Hours)**

General-purpose I/O, General-purpose Timers, Real-time Clock (RTC), Direct Memory Access (DMA), Analog-to-Digital Converter (ADC), Digital-to-Analog Converter (DAC), Serial Communication interface such as UART, I2C, SPI, Ethernet, CAN etc.

Total Contact Time: 45 Hours

3. Books Recommended

1. Joseph Yiu, “A definitive guide to the ARM-Cortex M3 and Cortex-M4 Processors”, 3rd Ed., Newnes, 2013
2. A. N. Sloss, D. Symes and C. Wright, “ARM System Developer’s Guide: Designing and Optimizing System Software”, Elsevier, 2004
3. Y. Zhu, “Embedded Systems with Arm Cortex-M3 Microcontrollers in Assembly Language and C”, E-Man Press LLC, 2014
4. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design (The Morgan Kaufmann Series in Computer Architecture and Design)”, 2nd Edition, 2008
5. Prasad K. V. K. K., “Embedded / Real-Time Systems: Concepts, Design And Programming”, DreamTech Press, 2005

M. Tech. I (VLSI & Embedded Systems) Semester – I SEMICONDUCTOR IC TECHNOLOGY ECVL111	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand material processing techniques and Pattern Transfer process
CO2	Demonstrates the concept behind thin film deposition, and characterization techniques.
CO3	Compare metal contact formation, interconnect, bonding and packaging.
CO4	Evaluate different fabrication, characterization, and metallization techniques.
CO5	Design basic semiconductor devices and their characterization.

2. Syllabus

INTRODUCTION TO MICROELECTRONIC FABRICATION AND MATERIALS **(08 Hours)**

Semiconductor substrate: Crystal structure, Crystal defects, Crystal growth, Wafer fabrication and basic properties of Silicon Wafers, Wafer cleaning, and native oxide removal, Substrates beyond Silicon, Surface reactions, Dopants, Defects in epitaxial growth, Clean Room, and Safety requirements. Diffusion, Thermal Oxidation, Ion implantation, Etching.

MASK FABRICATION AND ADVANCED LITHOGRAPHY TECHNIQUES **(05 Hours)**

Overview, Optical lithography, Photoresist, Mask Development, Patterning Strategies, Electron beam lithography process, EUV Lithography, X-ray lithography, and Other advanced lithography systems

THIN-FILM TECHNOLOGIES **(09 Hours)**

Physical Vapor Deposition: Evaporation Systems, Sputtering systems, and state-of-art Systems
Chemical Vapor Deposition: CVD system, Advanced CVD systems: LPCVD, UHCVD, AACVD, and advanced systems
Epitaxial Deposition: MOCVD, MBE, and CBE.
Solution-Based Deposition Techniques: Electrodeposition, Spin Casting, Printing, Layer-by-Layer Deposition, Colloidal Synthesis.

MEMS FABRICATION TECHNIQUES **(05 Hours)**

Silicon Pressure Sensors, Micro-Electro-Mechanical Systems, Micromachining Techniques, Isotropic Etching and Anisotropic Etching, Wafer Bonding, and LIGA Processes.

NANOSCALE DEVICE CHARACTERIZATION TECHNIQUES **(09 Hours)**

X-ray diffraction, X-ray photoelectron Spectroscopy, Spectroscopic Ellipsometry, Field Emission Scanning Electron Microscope, Transmission Electron Microscope, Atomic Force Microscope, Raman Spectroscopy, UV-Vis Measurement, Photo-Luminescence, Hall Measurement, Capacitance Voltage Measurement and Current-voltage measurement.

PROCESS INTEGRATION **(04 Hours)**

Contacts and metallization: Junction and oxide isolation, Si on insulator, Schottky and Ohmic contacts, Multilevel metallization.
CMOS technologies: Device behavior, Basic 3 μm technologies, Device scaling.
Circuit Manufacturing: Yield, Particle control, Design of experiments, computer-integrated manufacturing.

INTERCONNECTS, BONDING, AND PACKAGING: **(05 Hours)**

Metallization, Silicides, CVD Tungsten Plug Process, Gold Wire Bonding and Other Bonding Technologies, Package Types, Assembly Techniques, Package Fabrication Technology, Package Design Considerations.

(Total Contact Hours: 45)

3. Books Recommended

1. Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication”, 2nd edition Oxford University Press, 2006.
2. S. M. Sze (Ed), “VLSI Technology”, McGraw Hill, 1998.
3. Hrundle, Evans, Wilson, “Encyclopedia of Material Characterization”, Elsevier, 2005
4. D. K. Schroder, “Semiconductor Material and Device Characterization”, Wiley, 3rd edition, 2006
5. James Plummer, M. Deal and P. Griffin, “Silicon VLSI Technology”, Prentice Hall, 2016.
6. Rebeiz, G. M., RF MEMS: Theory Design and Technology, Wiley, 2004
7. Stephen A. Campbell, “Fabrication engineering at the Mocto- and NanoScale”, 4th edition Oxford University Press, 2013.

Additional Resources

1. Relevant Journals and Conference publications.

M. Tech. I (VLSI & Embedded Systems) Semester – I HARDWARE DESCRIPTION LANGUAGE ECVL113	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the concept of structural, data flow and behavioral style of hardware description and model various delays
CO2	Implement register transfer and gate level Digital system circuits. Also, verify with HDL simulations, Sequential circuits and FSMs
CO3	Develop and implement combinational logic circuits such as mux, demux, encoder, decoder, adders using Verilog and VHDL.
CO4	Evaluate the synthesized hardware for area, power and speed
CO5	Design ALU, instruction decoder, FIFO using HDL

2. Syllabus

INTRODUCTION **(11 Hours)**

Basic Concepts Of Hardware Description Languages, Hierarchy, Concurrency, Logic And Delay Modeling, Structural, Data-Flow And Behavioral Styles of Hardware Description, Architecture Of Event Driven Simulators

VHDL – Modelling and Analysis **(16 Hours)**

Syntax And Semantics Of VHDL, Variable And Signal Types, Arrays And Attributes, Operators, Expressions And Signal Assignments, Entities, Architecture Specification And Configurations, Component Instantiation, Concurrent And Sequential Constructs, Use Of Procedures And Functions, Examples of Digital Design Using VHDL

VERILOG – Digital Design and Synthesis **(18 Hours)**

Syntax And Semantics Of Verilog, Variable Types, Arrays And Tables, Operators, Expressions And Signal Assignments, Modules, Nets And Registers, Concurrent And Sequential Constructs, Tasks And Functions, Examples Of Design Using Verilog, Synthesis Of Logic From Hardware Description

(Total Contact Hours: 45)

3. Books Recommended

1. Bhaskar J.,“VHDL Primer”,Pearson Education Asia, 3rd Edition, 2015
2. Perry D.,“VHDL”,Tata McGraw-Hill, 4th Edition, 2017
3. Navabi Z.,“VHDL”,McGraw Hill, 3rd Edition,2007
4. Palnitkar S.,“Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson, 2nd Edition, 2003
5. Bhaskar J.,“Verilog HDL Synthesis - A Practical Primer”,Star Galaxy Publishing, 2018

M. Tech. I (VLSI & Embedded Systems) Semester – I PROCESSOR ARCHITECTURE ECVL115	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Discuss different processor architectures and system-level design processes.
CO2	Demonstrate the components and operation of a memory hierarchy and the range of performance issues influencing its design.
CO3	Analyze the organization and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
CO4	Evaluate the principles of I/O in computer systems, including viable mechanisms for I/O and secondary storage organization.
CO5	Develop systems programming skills in the content of computer system design and organization.

2. Syllabus

COMPUTER ABSTRACTIONS AND TECHNOLOGY (04 Hours)

Technologies for building processors and memory, Performance, Power wall, the switch from uniprocessors to Multiprocessors.

INSTRUCTION SET ARCHITECTURE OF 64-BIT RISC-V (08 Hours)

RISC-V addressing modes, instruction types, logical operations, instructions for making decisions, supporting procedures, RISC-V addressing for Wide Immediate and addresses, parallelism and instructions, comparison with MIPS and x86 Architectures.

PIPELINING (11 Hours)

An overview of pipelining, pipelined data-path and control, Data hazards: Forwarding versus Control, Control hazards, Exceptions, Parallelism via instructions, Real stuff: ARM Cortex-A53 and Intel Core i7 Pipelines, Case study: ILP and matrix multiply.

PARALLEL PROCESSORS (13 Hours)

Parallel programs, Flynn's taxonomy, Hardware multithreading, multicore and shared memory multiprocessors, Graphics processing units, Clusters and message passing multiprocessors, Multiprocessor networks, Benchmarking of Intel Core i7 960 and NVIDA Tesla GPU, Case study: Multiprocessors and matrix multiply, Cache coherence, Advanced Cache optimizations, Real stuff: The ARM Cortex-A53 and Intel Core i7 memory hierarchy, Case study: Cache blocking and matrix multiply.

STORAGE AND INTERCONNECTION (09 Hours)

The basic principles of interconnection network design, On-Chip Interconnection Network, Router Architecture, Network interface design, Case Study: NoC

(Total Contact Hours: 45)

3. Books Recommended

1. David A. Patterson, John L. Hennessy, “Computer Organization and Design: The Hardware Software Interface [RISC-V Edition]”, The Morgan Kaufmann Series in Computer Architecture and Design, 2017
2. John L Hennessy, “Computer architecture: a quantitative approach”, 6th Ed., Morgan Kaufmann Publishers, 2019
3. Leander Seidlitz, "RISC-V ISA Extension for Control Flow Integrity", Technische Universität München, 2019
4. Andrew Waterman, KrsteAsanović, The RISC-V Instruction Set Manual: Volume I: User-Level ISA, riscv.org, 2017
5. Andrew Waterman, KrsteAsanović, The RISC-V Instruction Set Manual: Volume II: Privileged Architecture, riscv.org, 2017

4. Reference Books

1. William James Dally, Brian Patrick Towles, “Principles and Practices of Interconnection Networks”, Morgan Kaufmann, Year: 2004

M. Tech. I (VLSI & Embedded Systems) Semester – I TESTING AND VERIFICATION OF VLSI CIRCUITS ECVL117	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand test patterns required to detect faults in a circuit
CO2	Demonstrate the testability of a circuit
CO3	Implement methods/techniques to improve the testability of digital circuits
CO4	Analyse Logic BIST circuits
CO5	Design the formal verification techniques

2. Syllabus

INTRODUCTION **(08 Hours)**

Scope Of Testing And Verification In VLSI Design Process, Issues In Test And Verification Of Complex Chips, Embedded Cores And SOCs

VLSI TESTING OF FAULT MODELS **(20 Hours)**

Fundamentals Of Automatic Test Pattern Generation, Design For Testability, Scan Design, Test Interface And Boundary Scan, System Testing and Test For SOC, Delay Fault Testing

Mu TESTING OF LOGIC AND MEMORIES **(10 Hours)**

Test Automation, Design Verification Techniques Based On Simulation, Analytical And Formal Approaches

VERIFICATION **(07 Hours)**

Functional Verification, Timing Verification, Formal Verification, Basics of Equivalence Checking And Model Checking, Hardware Emulation

(Total Contact Hours: 45)

3. Books Recommended

1. Bushnell M. and Agrawal V. D.,“Essentials Of Electronic Testing For Digital, Memory And Mixed-Signal VLSI Circuits”,Kluwer Academic Publishers,2013.
2. Abramovici M., Breuer M. A. and Friedman A. D.,“Digital Systems Testing And Testable Design”,IEEE Press,1990.
3. Erik Seligman, Tom Schubert and M V Achutha Kiran Kumar, “ Formal Verification An Essential Toolkit for Modern VLSI Design ”, Morgan Kaufmann Publisher, 2023
4. Rashinkar P., Paterson and Singh L.,“System-On-A-Chip Verification-Methodology And Techniques”,Kluwer Academic Publishers,2001.
5. Neil H. E. Weste and David Harris,“Principles Of CMOS VLSI Design”,Addison Wesley, 3rd Edition,2004

M. Tech. I (VLSI & Embedded Systems) Semester – I NANOELECTRONICS ECVL119	Scheme	L	T	P	Credit
		3	0	0	03

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Define various carrier transport mechanisms, properties of semiconductor materials, and novel devices using mathematical equations.
CO2	Describe the physics needed for special classes of nanoelectronic devices and their applications.
CO3	Illustrate the working of various nanoelectronic devices.
CO4	Analyse various nanoelectronic devices.
CO5	Design novel devices, processes, and applications based on them.

2. Syllabus

FUNDAMENTALS OF NANOSCALE PHYSICS **(12 Hours)**

Top-Down and Bottom-Up Approach, Potential of Nanotechnology and Nanoelectronics, Classical Particles, Quantum Mechanics of Electrons, Free and Confined Electrons, Quantum Structures.

BAND THEORY OF SOLIDS **(08 Hours)**

Electrons in Periodic Potential, Kronig-Penney Model of Band Structure, Band Theory of Solids, Graphene and Carbon Nanotubes.

TUNNEL JUNCTION AND APPLICATIONS OF TUNNELING **(07 Hours)**

Tunnelling Through a Potential Barrier, Potential Energy Profiles for Material interfaces, Applications of Tunnelling: Field Emission, Gate-Oxide Tunnelling and Hot Electron Effects in MOSFETS, STM and Double Barrier Tunnelling, and The Resonant Tunnelling Diode.

COULOMB BLOCKADE AND THE SINGLE-ELECTRON TRANSISTOR **(07 Hours)**

Coulomb Blockade: Coulomb Blockade in a Nanoscale capacitor, Tunnel Junctions, Tunnel Junction Excited by a Current Source, and Coulomb Blockade in Quantum dot circuit, Single-Electron Transistor.

QUANTUM STRUCTURES **(11 Hours)**

Quantum Wells, Quantum Wires and Quantum Dots, Ballistic Transport and Spin Transport.

(Total Contact Hours: 45)

3. Books Recommended

1. Hanson G. W., “Fundamentals of Nanoelectronics”, 1st Ed., Pearson Education, 2009.
2. Rogers B., Adams J. and Pennathur S. , “Nanotechnology: Understanding Small Systems”, CRC Press, Tayler and Francis Group, Third Edition, 2014.
3. Mahalik N. P., “Micromanufacturing and Nanotechnology”, Springer, 2006.
4. Kohler M., and Fritzsche W. , “Nanotechnology: An Introduction To Nanostructuring Techniques”, 1st Edition, 2008.
5. Kittel C., “Introduction to Solid State Physics”, Wiley, Eighth Edition, 2005.

M. Tech. I (VLSI & Embedded Systems) Semester – I ADVANCED MATERIAL CHARACTERIZATION TECHNIQUES ECVL121	Scheme	L	T	P	Credit
		3	0	0	03

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Describe and analyze different techniques available for the structural characterization of various materials systems.
CO2	Demonstrate knowledge of optical and electron microscopic techniques (microstructure imaging) to characterize different materials.
CO3	Analyze the internal structure of the material systems with different advanced diffraction techniques.
CO4	Evaluate appropriate spectroscopic techniques to measure electronic transitions to estimate parameters like energy band gap, elemental concentration, etc.
CO5	Investigate different characterization techniques in materials research and applications

2. Syllabus

INTRODUCTION **(05 Hours)**

Materials Properties and Microstructures, Need of materials characterization and available techniques, Probing Mechanisms for Materials Analysis

OPTICAL MICROSCOPY **(10 Hours)**

Optical microscope - Basic principles and components, Different examination modes (Bright field illumination, Oblique illumination, Dark field illumination, Phase contrast, Polarised light, Hot stage, Interference techniques), Stereomicroscopy, Photo-microscopy, Colour metallography.

ELECTRON MICROSCOPY **(10 Hours)**

Interaction of electrons with solids, Scanning electron microscopy Transmission electron microscopy and specimen preparation techniques, Scanning transmission electron microscopy, Energy dispersive spectroscopy, Wavelength dispersive spectroscopy.

ADVANCED DIFFRACTION TECHNIQUES **(08 Hours)**

Fundamental crystallography, Generation and detection of X-rays, Diffraction of X-rays, X-ray diffraction techniques, Electron diffraction.

ADVANCED SPECTROSCOPIC TECHNIQUES **(12 Hours)**

Optical Spectroscopy: UV, visible, IR, and Raman spectroscopes
Electron spectroscopy: Importance of surface characterization techniques, Physical principles of XPS, Photoelectric effects, XPS, AES & SIMS, Instrumentation, XPS patterns, Spin orbital Splitting, Quantitative analysis, Chemical effect, Chemical shift, Auger electron generation, Chemical effect, Quantitative analysis, Depth profiling and Applications

(Total Contact Hours: 45)

3. Books Recommended

1. C. S. Kumar, M. M Singh, R. Krishna, “Advanced material characterization”, 1st Edition CRC Press, Taylor and Francis Group, 2023
2. Sam Zhang, Lin Li, and Ashok Kumar “Materials Characterization Techniques”,1st Edition, CRC Press, 2008
3. A. K. Tyagi, Mainak Roy, S. K. Kulshreshtha and S. Banerjee, “Advanced Techniques for Materials Characterization”, Materials Science Foundations (monograph series), Volumes 49 – 51, 2009
4. P. R. Khangaonkar, “Introduction To Materials Characterization”, 1st Edition, Penram Intl. Publishing (India) Pvt. Ltd, 2008
5. D. Briggs, J.T. Grant (eds.), “Surface analysis by Auger and X-ray photoelectron spectroscopy”, IM Publications and Surface Spectra Limited, Cromwell Press, Trowbridge, UK, 2003

M. Tech. I (VLSI & Embedded Systems) Semester – I ADVANCE DSP ECCS105	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Define different type of signals and systems, and analyze different system characteristics therein
CO2	Describe the concept of FIR, IIR, linear prediction filter, power spectrum estimation
CO3	Solve the problem related to different filtering techniques and power spectrum estimation
CO4	Analyze different filtering techniques
CO5	Design different filtering techniques for different signal processing applications

2. Syllabus

REVIEW OF DISCRETE SIGNAL REPRESENTATION AND ANALYSIS (06 Hours)

Continuous and discrete time signals, noise signal, different type of signals, operations of signals: addition, subtraction, multiplication, scaling, magnification, decimation, interpolation, differentiation and integration, static and dynamic system, LTI system, DFT and FFT

TIME AND FREQUENCY-DOMAIN DESIGN TECHNIQUES FOR IIR AND FIR FILTERS (09 Hours)

FIR And IIR Filter Specifications, FIR Filter Design- Fourier series method and Frequency Sampling Method, Design Of IIR Digital Filters: Butterworth, Chebyshev And Elliptic Approximations, Low Pass, Band Pass, Band Stop And High Pass Filters, Bilinear Transformation Method

EFFECT OF FINITE REGISTERS LENGTH (04 Hours)

Number Representation, Quantization Error, Round-Off Error, Overflow Error, Limit Cycle, System Noise behaviour, Noise Filtering By LSI System, Noise in a Cascade Of 2nd Order Filter, Stability of Linear Filter

MULTIRATE SIGNAL PROCESSING (05 Hours)

General Rate-Changing System, Integer-Factor Interpolation and Decimation and Rational-Factor Rate Changing, Efficient Multirate Filter Structures, Over sampling D/As, Perfect-Reconstruction Filter Banks and Quadrature Mirror Filters.

OPTIMAL FILTERING OF RANDOM SIGNALS (08 Hours)

Innovations Representation of a Stationary Random Process, Prediction, linear prediction: forward and backward methods, Linear prediction based filter analysis, Prediction error, Levinson recursion method for solving Toeplitz system of equations, AR and ARMA Filter, MLE and MAP, LMS and RLS adaptive filters.

POWER SPECTRUM ESTIMATION/ANALYSIS (06 Hours)

Non-parametric method, Parametric method, periodogram, Eigen analysis for spectral Estimation.

APPLICATION OF DSP **(07 Hours)**

Speech signal processing: Time domain processing of speech, methods for extracting the parameters, Filter bank analysis of speech, radar signal processing, musical sound processing, recent applications.

(Total Contact Hours: 45)

3. Books Recommended

1. Salivahanan S, “Digital Signal Processing”, Fourth Edition, Tata McGraw-Hill, 2019.
2. Rabiner L. R. and Gold B., “Theory and Applications Of Digital Signal Processing”, First Edition, Prentice Hall, 1992.
3. Oppenheim A. V. and Schafer, “Discrete Time Signal Processing”, Pearson, Third edition, 2014.
4. Proakis John G. and Manolakis D.G., “Digital Signal Processing: Principle, Algorithms and Applications”, Fourth Edition, Pearson, 2006.
5. Kay, Steven M “Fundamentals of statistical signal processing”, Prentice Hall, 1998.
6. L. R. Rabiner and R. W. Schafer, Digital Processing of Speech Signals, Pearson Education India, First Edition, 2003.

4. Reference Books

1. Mitra Sanjit K.,“Digital Signal Processing - A computer Based Approach”, McGraw-Hill,2005

M. Tech. I (VLSI & Embedded Systems) Semester – I INFORMATION THEORY AND CODING ECCS111	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the notion of information in a mathematically sound way.
CO2	Compare and analyze lossless data compression techniques with varying efficiencies as per problem requirements.
CO3	Calculate entropy, joint entropy, relative entropy, conditional entropy, and channel capacity of a system.
CO4	Design decoding strategies for block codes, linear codes, cyclic codes and BCH codes for detection and correction of errors.
CO5	Design convolutional Encoding and Decoding that meets design objectives like required protection for detection and correction of errors.

2. Syllabus

INFORMATION THEORY (06 Hours)

Introduction to Information Theory, Entropy, Properties of Entropy, Measures for Continuous, Random Variable, Relative Entropy, Conditional and Joint Entropy, Measure of Information, Average Information, Extension of Zero Memory Source.

SOURCE CODING (12 Hours)

Properties of Codes, Variable Length Codes, Uniquely Decodable Codes, Kraft's Inequality, Prefix Codes, Average Length of a Code, Shannon's First Theorem, Shannon's Encoding Algorithm, Shanon-Fano Codes, Huffman's Codes, Arithmetic Codes, Lempel Ziv, Run Length Code, Code Efficiency and Redundancy, Practical Application of Source Coding: JPEG Compression.

CHANNEL MODELS AND CHANNEL CAPACITY (08 Hours)

Discrete Communication Channels, Continuous Channels, Entropy Functions and Equivocation, Mutual Information, Channel Capacity, redundancy and efficiency of channels, Symmetric channels, Binary Symmetric Channel, Binary Erasure Channel, Noise-Free Channel, Cascaded channels, Binary asymmetric channel, Shannon theorem

BLOCK CODES AND LINEAR CODES (06 Hours)

Introduction to Galois Field, Single Parity Check Codes, Product Codes, Hamming Codes, Minimum Distance of Block Codes, Linear Block Codes, Generator Matrices, Parity Check Matrices, Encoder, Standard array and Syndrome decoding, Error Correction and Error Detection Capabilities.

CYCLIC and BCH CODES **(08 Hours)**

Introduction to Cyclic Codes, Generator Polynomial, Syndrome Polynomial and Matrix Representation, Fire Code, Golay Code, CRC Codes and Circuit Implementation of Cyclic Codes, Introduction to BCH Codes: Generator Polynomials, Multiple Error Correcting BCH Codes, Decoding of BCH Codes, Introduction to Reed Solomon (RS) Codes.

CONVOLUTION CODE **(05 Hours)**

Introduction to Convolutional Codes, Trellis Codes: Generator Polynomial Matrix and Encoding using Trellis, Vitrebi Decoding, Introduction to Turbo Codes, Introduction to Trellis Coded Modulation (TCM), Introduction to Space Time Block Codes (STBC).

(Total Contact Hours: 45)

3. Books Recommended

1. Ranjan Bose, “Information theory, coding and cryptography”, Tata McGraw-Hill,2nd Edition, 2008
2. T. M. Cover and J. A. Thomas, “Elements of Information Theory“, 2nd Ed., John Wiley & Sons,
3. New Jersey, USA, 2006.
4. Salvatore Gravano, “Introduction to Error Control Codes”, Oxford University Press,1st Edition, 2007
5. Shu Lin and Daniel Costello, “Error Control Coding”, 2nd Ed., by Pearson, 2004.
6. Todd K. Moon, “Error Correcting Coding”, Wiley India Edition,2006

M. Tech. I (VLSI & Embedded Systems) Semester – I MACHINE LEARNING AND APPLICATIONS ECCS121	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand fundamentals of Machine Learning and classify machine learning algorithms into supervised and unsupervised.
CO2	Evaluate performance of different ML algorithms and select suitable algorithm for a given problem.
CO3	Analyze a given problem and determine which algorithm to use.
CO4	Solve problems using various machine learning techniques.
CO5	Design applications using various ML algorithms to solve real life problems.

2. Syllabus

INTRODUCTION TO MACHINE LEARNING AND PREREQUISITES (11 Hours)

Definition and history of machine learning, Types of Machine Learning: Supervised, Unsupervised, and Reinforcement Learning, Applications of Machine Learning, Essential mathematics for machine learning: linear algebra and probability theory, Bayesian learning, Naïve Bayes, Normal density and discriminant function.

SUPERVISED MACHINE LEARNING ALGORITHMS (13 Hours)

Regression: Linear regression, Multiple linear regression, Polynomial regression, Ridge regression, Lasso Regression. **Classification:** Perceptron criteria, Logistic Regression, Multi-class logistic regression (one-vs-all), K-nearest neighbours (KNN), Linear support vector machine (SVM), Kernel SVM, Linear Machine with hinge loss, Decision trees and random forests.

UNSUPERVISED MACHINE LEARNING ALGORITHMS (12 Hours)

Clustering: K-Means clustering, Fuzzy K-means clustering, Mean shift clustering, Hierarchical clustering, DBSCAN, Gaussian mixture model, Expectation Maximization Algorithm. **Dimensionality Reduction:** Dimensionality Problem, Principal component analysis (PCA), t-Distributed Stochastic Neighbour Embedding (t-SNE), Linear Discriminant Analysis (LDA). Anomaly Detection.

INTRODUCTION TO DEEP LEARNING (09 Hours)

Neural Networks: Biological Neurons vs. Artificial Neurons, Perceptron, Learning XOR, Multilayer perceptron (MLP), Feed forward neural networks, Activation Functions: Sigmoid, Tanh, ReLU, etc. **Training Neural Networks:** Forward and backward propagation, Gradient Descent, Optimization algorithms, Loss functions, Overfitting and Regularization (Dropout, Batch Normalization). **CONVOLUTIONAL NEURAL NETWORKS:** Convolution, Cross correlation, building blocks of CNN, MLP vs CNN, Popular CNN models, Vanishing and Exploding Gradient.

Total Contact Time = 45 Hours

3. Books Recommended

1. C. M. Bishop, Pattern Recognition and Machine Learning, Springer, 2nd Ed., 2011.
2. Kevin P. Murphy, Machine Learning: A Probabilistic Perspective, The MIT Press, 2012.
3. Ethem Alpaydin, Introduction to Machine Learning, The MIT Press, 4th Ed, 2020.
4. Mehryar Mohri, Afshin Rostamizadeh, Ameet Talwalkar, Foundations of Machine Learning, The MIT Press, 2nd Ed, 2018.
5. Ian Goodfellow, Yoshua Bengio and Aaron Courville, Deep Learning, MIT Press, 2016.

M. Tech. I (VLSI & Embedded Systems) Semester – I VLSI LAB – I ECVL107	Scheme	L	T	P	Credit
		0	0	6	03

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Understand the Semiconductor Devices, IC Technology, Digital VLSI Design and HDL
CO2	Implement the Semiconductor Devices, IC Technology, Digital VLSI Design
CO3	Analyze the Semiconductor Devices, IC Technology, Digital VLSI Design
CO4	Evaluate the performance the Semiconductor Devices, IC Technology, Digital VLSI Design
CO5	Design the Digital VLSI circuits for the given parameter using circuit at circuit level and at RTL

Semiconductor IC Technology

Following is the list of experiments but not limited to:

1. Demonstration of processing steps involved in the cleaning of Silicon wafers.
2. Demonstration of different furnaces used in material processing such as Muffle Furnace, vacuum oven, etc.,
3. Demonstration of microfabrication processes like deposition (Thermal Evaporation, DC Sputtering, RF Sputtering, etc.), patterning, etc.
4. Demonstration of Chemical Deposition Process for the material growth (Chemical Vapor Deposition, Spin Coating, etc.)
5. Electrical properties estimation of the thin film materials using Four Probe Hall Effect measurement setup.
6. Demonstration of spectrometers (Raman Spectrometer, UV-Visible-NIR Spectrometer
7. Current-Voltage and Capacitance-Voltage characteristics measurement using semiconductor parameter analyzer for different semiconductor devices.
8. Design a semiconductor resistor and simulate it for its current voltage characteristics.

MOS Device Technology

1. Simulate p-n junction diodes, plot current-voltage characteristics under forward and reverse bias and extract key parameters.
2. Simulate MOS Capacitor, plot capacitance-voltage characteristics and extract the key parameters.
3. Simulate n-Channel MOSFET, plot transfer and output characteristics. Extract critical parameters i.e. V_T, g_m, r_d, subthreshold slope (SS), etc. Show structural analysis using electron density and energy band diagram.
4. Simulate p-channel MOSFET. Plot transfer and output characteristics. Extract critical parameters i.e. V_T, g_m, r_d, subthreshold slope (SS), etc. Show structural analysis using electron density and energy band diagram.
5. CMOS inverter design and layout for given static and dynamic specifications.
6. CMOS Combinational Logic gate design and layout for given static and dynamic specifications.

Digital VLSI Design

1. CMOS inverter design and layout for given static and dynamic specifications
2. CMOS Combinational Logic gate design and layout for given static and dynamic specifications
3. Pass transistor and Transmission gate based logic design and layout
4. CMOS latches and Flip Flop design and layout
5. Dynamic logic circuit design and layout
6. CMOS logic circuit design using logical efforts
7. Design and layout of memory cells and sense amplifiers
8. Design and layout of adders - Ripple carry, Manchester carry, carry look ahead, carry select and carry save using full custom flow and find the area-delay product and power-delay product.
9. Design and layout of multipliers - Array, carry save, Wallace tree structures using full custom flow and find the area-delay product and power-delay product.
10. Design and layout of shifters and floating point arithmetic units using full custom design and find the area-delay product and power-delay product.

Embedded Systems

1 Introduction to ARM Cortex M3/M4 evaluation board and Keil ARM – MDK development flow.

2 Write an program to flash simple LEDs (D0, D1, ... , D7) connected to Ports in various Patterns

3 Write code to show up/down BCD count on Multiplexed 7-segment LED display updated every second. Use two keys (up & down) to change direction of counting.

4 Write a program to display “Welcome to SVNIT” as welcome message on LCD interface.

5 Interface 4x4 keypad and Display pressed key on LCD.

6 Interface stepper motor and rotate it in clockwise and anti-clock wise direction.

7 Generate Sine wave/Triangle/Square wave using SPI based DAC and observe on CRO. Increase or Decrease frequency using Keys in decades

8 Using the internal PWM module of ARM microcontroller, generate PWM and vary its duty cycle to control DC motor.

9 Interface accelerometer and read the its output through I2C serial communication.

10 Illustrate use of CMSIS-RTOS functions for embedded programming.

11 Demonstrate the use of keil RTX real time operating system for toggling LED ON/OFF.

12 Demonstrate use of threads and semaphores using keil RTX RTOS

HDL

1. Implement Behavioral, Data flow and structural Modeling
2. Realization of combinational and sequential design style
3. Realization of blocking and non-blocking assignment statements
4. Realization of signal vs variable
5. Implementation of Testbench and debugging concept
6. Implementation of state machine
7. ALU design using state machine
8. Logic implementation on FPGA board

M. Tech. I (VLSI & Embedded Systems) Semester – I Seminar ECVL109	Scheme	L	T	P	Credit
		0	0	4	02

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Understand any topic of interest and develop a thought process for technical presentation
CO2	Demonstrate a detailed literature survey and build a document with respect to technical publications.
CO3	Analyze the proof-of-concept and related data.
CO4	Evaluate the presentation skill.
CO5	Create technical reports

M. Tech. I (VLSI & Embedded Systems) Semester – II ANALOG VLSI DESIGN ECVL102	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand Impact of MOS Device Parameters on Analog Circuit Design and the Analog Design Requirements.
CO2	Design and Analyze various CMOS Amplifiers, Differential Amplifiers, Current Source/Sink Circuitry.
CO3	Analyze various Op-amp topologies and compensation techniques.
CO4	Evaluate suitability of a specific topology of Analog Sub-Circuits / Biasing Circuits / Data Converters etc. for a particular application.
CO5	Investigate Switch Capacitor Circuits for filter design

2. Syllabus

ANALOG CMOS SUB-CIRCUITS (10 Hours)

Small Signal Model For MOS, MOS Switch, MOS Resistors, Current Sink/Source, High Input Impedance Current Mirrors, Differential, Cascode And Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures

CMOS OPERATIONAL AMPLIFIERS (09 Hours)

Design of CMOS Operational Amplifiers, Telescopic Op-amp topologies, Compensation, Design of Two Stage Op-Amps, Cascode Op-Amps, Simulation And Measurement Techniques

HIGH PERFORMACE CMOS OP-AMPS (07 Hours)

Buffered Op-Amps, High Speed/Frequency Op-Amps, Differential Output Op-Amps, Micro Power Op- Amps, Low Noise And Low Voltage Op-Amps

SWITCHED CAPACITOR FILTERS (09 Hours)

Switched Capacitor Circuits: Design and Analysis, Switched Capacitor Amplifiers, Switched Capacitor Integrators, Z Domain Models, 1st And 2nd Order Switch Capacitor Filters, Higher Order Filters

D/A AND A/D CONVERTERS (10 Hours)

Sample And Hold Circuits. Characterization of DAC, Nyquist Rate, Parallel DAC, Extending Resolution Of Parallel DAC, Serial DAC, Characterization Of ADC, Serial ADC, High Speed ADC, Over Sampling Techniques

Total Contact Time: 45 Hours

3. Books Recommended

1. John D. A. and Martin K., “Analog Integrated Circuit Design”, 2nd Ed., Wiley, 2013
2. Razavi Behzad, “Design of Analog CMOS Integrated Circuit”, Tata McGraw-Hill, 2nd Edition, 2017
3. Allen Philip and Holberg Douglas, “CMOS Analog Circuit Design”, Oxford University Press, 3rd Edition, 2016
4. Gregorian R. and Temes G.C., “Analog MOS ICs for Signal Processing”, Wiley 2008
5. Baker Jacob R., Harry W. Li and Boyce David E.,“CMOS: Circuit Design, Layout and Simulation”, Wiley, Interscience, 3rd Edition, 2013

M. Tech. I (VLSI & Embedded Systems) Semester – II REAL TIME SYSTEMS ECVL104	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe the foundation for programming languages developed for real time programming.
CO2	Apply real time operating systems and their functions.
CO3	Analyze the real time network.
CO4	Evaluate the real time systems with regard to keeping time and resource restrictions.
CO5	Design real time applications with RTOS.

2. Syllabus

INTRODUCTION TO REAL-TIME SYSTEMS (09 Hours)

Hard versus Soft Real Time Systems, Reference Models of Real Time Systems, Operating System Services, I/O Subsystems, Network Operations Systems, Real Time Embedded Systems, Operating Systems Interrupt Routines in RTOS Environments, RTOS Task Scheduling Models, Interrupt Latency and Response Time, Standardization Of RTOS

REAL-TIME SCHEDULING AND SCHEDULABILITY ANALYSIS (10 Hours)

Task, Process and Threads, Commonly Used Approaches To Real Time Scheduling, Clock-Driven Scheduling, Priority Driven Scheduling Of Periodic Tasks, Hybrid Scheduler, Event Driven Schedules, Earliest Dead Line First (EDF) Scheduling, Rate Monotonic Algorithm (RMA), Real Time Embedded Operating Systems: Standard & Perspective, Real Time Operating Systems: Scheduling Resource Management Aspects, Quasi-Static Determining Bounds On Execution Times

RESOURCE SHARING AMONG REAL-TIME TASKS (12 Hours)

Data Sharing by Multiple Tasks And Routines Inter Process Communication, Handling Resources Sharing and Dependencies Among Real-time Tasks, Resource Sharing Among real Time tasks, Priority Inversion, Priority Inheritance Protocol (PIP), Highest Locker Protocol (HLP), Priority Ceiling Protocol (PCP), Different Types of Priority Inversion Under PCP, Important Features of PCP, Handling Task Dependencies,

DISTRIBUTED REAL-TIME SYSTEMS, MULTIPROCESSOR REAL-TIME SYSTEMS (07 Hours)

Multiprocessor and Distributed system, Partitioned scheduling, Global scheduling, Semi-partitioned scheduling, Distributed scheduling, Load balancing

REAL TIME COMMUNICATION AND DATABASE **(07 Hours)**

Real time traffic, Real-time data link layer, Protocols: CAN, Time-triggered protocol (TTP), Real-time ethernet, Real-time IEEE 802.11, Mobile Wireless Sensor Network

Total Contact Time: 45 Hours

3. Books Recommended

1. Rajib Mall, “Real Time Systems Theory and Practice”, 1st Ed., Pearson Education, 2007.
2. Brian Amos, “Hands-On RTOS with Microcontrollers: Building real-time embedded systems using FreeRTOS, STM32 MCUs, and SEGGER debug tools”, 1 st Edition, Packt Publishing, 2020
3. K. Erciyes, “Distributed Real-Time Systems-Theory and Practice”, Springer Cham, 1 st Edition, 2019
4. Liu Jane, “Real-time Systems”, 1 st Ed., Pearson Education, India, 2006.
5. Xiaocong Fan, “Real-Time Embedded Systems-Design Principles and Engineering Practices”, 1 st Edition, Newnes, 2015

M. Tech. I (VLSI & Embedded Systems) Semester – II SOLAR PHOTOVOLTAICS TECHNOLOGY ECVL170	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Explain Solar Resource and Basics of Photovoltaic Systems.
CO2	Describe requirements for the efficient Photovoltaic Device Design and Processing.
CO3	Demonstrate different solar cell fabrication and characterization techniques.
CO4	Analyze the Current and Emerging PV technologies, and PV Module related concepts.
CO5	Design the Solar Photovoltaic Devices and PV Modules

2. Syllabus

INTRODUCTION TO SOLAR PHOTOVOLTAICS (03 Hours)

Solar Resource, Solar Energy Conversion Technologies, Need of Solar PV, Prospects of PV technology.

FUNDAMENTALS OF SOLAR CELLS (10 Hours)

Light Absorption, Charge Excitation, Charge Drift/Diffusion, Charge Separation, Charge Collection, PN junction diodes: Dark IV, illuminated IV, Device Performance parameters: Short Circuit Current, Open Circuit Voltage, Fill Factor, Efficiency, Series/ Shunt Resistance, Factors affecting the performance parameters, Detailed Balanced Limit.

FABRICATION AND CHARACTERIZATION OF SOLAR CELLS (10 Hours)

Solar Cell Fabrication:

Vacuum Based Deposition Techniques: Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD): Sputtering, Electron Beam Evaporation, Pulsed Laser Deposition, Atomic Layer Deposition, Molecular Beam Epitaxy.

Solution Based Deposition Techniques: Electrodeposition, Spin Coating, Layer-by Layer Deposition, Printing, Colloidal Synthesis.

Solar Cell Characterization:

Solar Simulator, Quantum Efficiency Measurement, Secondary Ion Mass Spectroscopy, XPS/UPS, FESEM, Energy Dispersive X-Ray Spectroscopy, Photo-Luminescence

COMMERCIAL AND EMERGING TECHNOLOGIES IN SOLAR CELLS (10 Hours)

Silicon PV Technology, Chalcopyrite/ Kesterite Solar Cells, Organic Photovoltaics, Dye Sensitized Solar Cells, Perovskite Solar cells, Transparent Photovoltaic Devices, Flexible PV Devices, Multijunction Devices, Concentrator Solar Cells.

CUTTING-EDGE THEMES AND PV MODULES **(07 Hours)**

Light manipulation in PV Devices: Plasmonic Integration, Surface Texturing, Spectrum Splitting Techniques.

Module Design, Interconnection effects, Temperature effects, Lifetime of PV modules, Module measurement.

PV DEVICE MODELING **(05 Hours)**

Basics of Solar Cell Device Modeling, Thin-Film Solar Cell Device Modeling: Hands-on with an Open Source Tool, Modeling of PV Modules.

(Total Contact Hours: 45)

3. Books Recommended

1. Martin A. Green, “Solar Cells: Operating Principles, Technology and System Applications”,, Prentice-Hall, 1986.
2. Jenny Nelson, “The Physics of Solar cells”, World Scientific, 2003.
3. Smets Arno et al., “Solar Energy Fundamentals, Technology, and Systems”, UIT Cambridge. 2013
4. D. K. Schroder, “Semiconductor Material and Device Characterization”, Wiley Interscience, 2006
5. Konrad Mertens, “Photovoltaics Fundamentals, Technology, and Practice”, Wiley, 2018,
6. J. Poortmans and V. Arkhipov, “Thin Film Solar Cells: Fabrication, Characterization and Applications”, Willey, 2006.

4. Reference Recommended

1. Antonio Luque, Steven Hegedus, “Handbook of Photovoltaic Science and Engineering”, Wiley, 2011
2. Relevant Journal and Conference publications.

M. Tech. I (VLSI & Embedded Systems) Semester – II MEMS ECVL172	Scheme	L	T	P	Credit
		3	0	0	03

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Understand the MEMS fabrication process and characterization
CO2	Describe MEMS Materials & their Properties for Device Applications
CO3	Interpret Elasticity in Materials
CO4	Analyze MEMS Capacitive Switch
CO5	Design MEMS devices for different application

2 Syllabus:

INTRODUCTION TO MICRO-FABRICATION: (09 Hours)

Cleaning, Oxidation, Diffusion, Mask making, Lithography, Etching, Ion Implantation, CVD, PVD, Metallization; Surface micromachining and Bulk Micromachining, DRIE, LIGA, Fabrication of high aspect ratio deformable structures, wafer bonding

UNDERSTANDING MEMS MATERIALS & THEIR PROPERTIES FOR DEVICE APPLICATIONS (06 Hours)

Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson's ratio, density, piezoresistive coefficients, TCR, Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications

ELASTICITY IN MATERIALS (06 Hours)

Stress, strain calculations, Normal and Shear strains and constitutive relations, Plane stress, biaxial stress, residual stress, energy relations, Load-deflection calculations in beams, cantilevers (rectangular cross section), Elastic deformation in square plate, Resonant frequency calculations: Rayleigh-Ritz method

MEMS CAPACITIVE SWITCH (12 Hours)

Lumped model, pull-in voltage, Electromechanical deflection modeling, pull-in instability, switching time and pull-in voltage scaling, Physical effects in nanoscale gap-size, squeeze-film damping , perforated MEMS Capacitive switch, Comb actuators, Accelerometer, Pressure sensor, Energy approach: Lagrangian Mechanics applicable to MEMS capacitive switches, Reliability in RF-capacitive switch

MEMS DEVICES (09 Hours)

Architecture, working and basic quantitative behaviour of Cantilevers, Microheaters, Accelerometers, Pressure Sensors, Micromirrors in DMD, Inkjet printer-head. Thermal sensor design, Bio-MEMS, MEMS memory, Optical MEMS:2-D, 3-D switches.

MEMS DEVICE CHARACTERIZATION **(03 Hours)**

Piezoresistance, TCR, Stiffness, Adhesion, Vibration, Resonant frequency, Laser Doppler vibrometer, Electronic Speckle Interference Pattern technology (ESPI), and the importance of these measurements to study device behavior, MEMS Reliability.

3. Books Recommended

1. E. S. Kim, “Fundamentals of Microelectromechanical Systems (MEMS)”, McGraw Hill, 2021.
2. Tai–Ran Hsu, “Mems & Microsystems Design and Manufacturing”, John Wiley & Sons, 2nd Edition, 2008
3. Chang Liu, “Foundations of MEMS”, Pearson Education Inc., 2006.
4. Sandana A., “Engineering biosensors: kinetics and design applications”, Academic Press 2002
5. Marc J. Madou, “Fundamentals of Microfabrication”, 2nd Edition, CRC Press Taylor and Francis Group, 6000 Broken Sound Parkway NW, Suite 300, Boca Raton, FL33487- 2724, 2002.

4. Reference Recommended

1. Ville Kaajakari, “Practical MEMS”, Small Gear Publishing, 2009
2. S. Senturia “Microsystem Design”, 1st Edition, Springer, 2000
3. Minhang Bao, “Analysis and Design Principles of MEMS Devices”, 1st Edition, - Elsevier Science, 2005
4. J. Allen, “Micro Electro Mechanical System Design”, 1st Edition, CRC Press, 2005
5. G. Kovacs, “Micromachined Transducers Sourcebook”, 2nd Edition, McGraw-Hill, 2000

M. Tech. I (VLSI & Embedded Systems) Semester – II Foundation of VLSI CAD ECVL174	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand CAD tools used for VLSI design and synthesis
CO2	Optimize the algorithms for portioning in the design process of Complex IC
CO3	Demonstrate capability of floorplanning algorithm for CAD tool
CO4	Analyze various algorithms for Placement and Routing.
CO5	Investigate timing analysis and understand Timing Closure

2. Syllabus

INTRODUCTION TO VLSI CAD AND SYNTHESIS (06 Hours)

Intro to VLSI CAD & Logic Synthesis • Graph Theory & Optimization problems • Boolean Algebra • Boolean Function Representation & Manipulation: BDDs • Satisfiability & Graph Covering

NETLIST AND SYSTEM PARTITIONING (08 Hours)

Optimization Goals, Partitioning Algorithms: Kernighan-Lin (KL) Algorithm, Extensions of the Kernighan-Lin Algorithm, Fiduccia-Mattheyses (FM) Algorithm, A Framework for Multilevel Partitioning, Clustering, Multilevel Partitioning, System Partitioning onto Multiple FPGAs...

CHIP PLANNING (08 Hours)

Introduction to Floorplanning, Optimization Goals in Floorplanning, Floor Plan Representations, Floorplanning Algorithms, Pin Assignment, Power and Ground Routing

GLOBAL AND DETAILED PLACEMENT AND ROUTING (12 Hours)

Global Placement, Min-Cut Placement, Analytic Placement, Simulated Annealing, Modern Placement Algorithms, Legalization and Detailed Placement, The Global Routing Flow: Single-Net Routing; Rectilinear Routing; Global Routing in a Connectivity Graph; Finding Shortest Paths with Dijkstra's Algorithm; Finding Shortest Paths with A* Search, Full-Netlist Routing: Routing by Integer Linear Programming; Rip-Up and Reroute (RRR), Modern Global Routing: Pattern Routing; Negotiated Congestion Routing, Detailed Routing, Specialized Routing

TIMING CLOSURE (11 Hours)

Timing Analysis and Performance Constraints: Static Timing Analysis; Delay Budgeting with the Zero-Slack Algorithm, Timing-Driven Placement: Net-Based Techniques; Embedding STA into Linear Programs for Placement, Timing-Driven Routing: The Bounded-Radius, Bounded-Cost Algorithm; Prim-Dijkstra Tradeoff; Minimization of Source-to-Sink Delay, Physical Synthesis: Gate Sizing; Buffering; Netlist Restructuring

Total Contact Time: = 45 Hours

3. Books Recommended

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, “ VLSI Physical Design: From Graph Partitioning to Timing Closure ”, Springer Cham, 2023.
2. Khosrow Golshan, “ Physical Design Essentials ”, Springer New York, NY, 2010.
3. De Micheli, Synthesis and optimization of Digital Circuits, Tata McGraw Hill, 2003.
4. Sadiq M Sait, Habib Youssef, “ VLSI Physical Design Automation Theory and Practice “, , World Scientific Publishing Company, 1999
5. Naveed A. Sherwani, “ Algorithms for VLSI Physical Design Automation ”, Springer New York, NY, 2013

M. Tech. I (VLSI & Embedded Systems) Semester – II SEMICONDUCTOR DEVICE MODELLING ECVL176	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe semiconductor device physics and equations used for deriving a model.
CO2	Demonstrate various carrier transport equations.
CO3	Analyze methods to form closed-form analytical models.
CO4	Evaluate the operation of semiconductor devices using numerical methods.
CO5	Develop models for novel semiconductor devices.

2. Syllabus

DEVICE PHYSICS **(03 Hours)**

Review of Semiconductor Physics: PN Junction diode, Heterojunctions, MOSFETS.

SEMICONDUCTOR CARRIER TRANSPORT EQUATIONS **(07 Hours)**

The Boltzmann model, Maxwell's Equations, The Classical Semiconductor Equations, Boundary Conditions, Generation and Recombination, and Thermal Conductivity and Heat Flow.

CLOSED-FORM ANALYTICAL MODELS **(08 Hours)**

Solution Techniques for the Semiconductor Equations, Closed-Form Analysis of the Semiconductor Equations, Analysis of a PN junction diode, Analysis of Field effect Transistor Operation, Analysis of MOSFET Operation and Limitations of Closed-Form Analyses

FINITE-DIFFERENCE METHOD **(06 Hours)**

Finite-Difference Schemes, Discretization of the Semiconductor Equations, Methods of Solving the Finite-Difference Equations, Boundary Conditions, and Examples of Finite-Difference Simulations.

SEMICLASSICAL TRANSPORT EQUATIONS **(06 Hours)**

Hot Electron Effects: The Hydrodynamic Semi-classical Semiconductor Equations, Examples of Hot Electron Modelling

SIMULATION OF HETEROJUNCTION DEVICES **(05 Hours)**

Semiconductor Equations for Heterojunctions, High Electron Mobility Transistors: Closed-Form Models and Numerical Models.

THE MONTE CARLO METHOD **(05 Hours)**

The Monte Carlo Method applied to Carrier Transport in Semiconductors: Equations of Motion, Energy Band Structure and Free Flight, and Scattering Mechanisms, Treatment of Results, and Applications of Monte Carlo Simulations.

QUANTUM TRANSPORT THEORY **(05 Hours)**

Extension of Semiclassical Transport Concepts to Quantum Structures, Quantum mechanics – Basic Concepts, Application of Quantum Mechanics to Semiconductor Device Modelling, Quantum Transport Theory, and Applications of Quantum Transport Theory

Total Contact Time: = 45 Hours

3. Books Recommended

1. Snowden C.M., and, Snowden E., “Introduction to Semiconductor Device Modeling”, World-Scientific, 1998.
2. Selberherr S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag, First edition, 1984.
3. Taur Y. and Ning T.H. “Fundamentals of Modern VLSI Devices, “, Cambridge University Press, Third Edition, 2021.
4. Vasileska D., Goodnick S. M., and Klimeck G., “Computational Electronics Semiclassical and Quantum Device Modeling and Simulation, CRC Press, 2010.
5. Sze S. M., Li Y., and Kwok K. Ng, “Physics of Semiconductor Devices”, John Willey, Fourth Edition, 2021.

M. Tech. I (VLSI & Embedded Systems) Semester – II FUNDAMENTALS OF SEMICONDUCTOR PACKAGE MANUFACTURING AND TEST ECVL178	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe semiconductor package manufacturing processes.
CO2	Demonstrate various component and package test.
CO3	Analyze the electrical and physical failure in packaging.
CO4	Evaluate the semiconductor package materials and qualification.
CO5	Develop the strategies for industrial quality and statistical process control.

2. Syllabus

PACKAGE MANUFACTURING PROCESSES **(10 Hours)**

Packaging Assembly Technology, Wafer Thinning, Dicing, Die Attach, Wire bonding, Flip Chip process, Flux Cleaning, Underfill, Encapsulation, Laser Marking, Solder Ball Attach, Reflow, Singulation, IC Packaging Toolsets & equipment operation, clean room operations

SEMICONDUCTOR COMPONENT AND PACKAGE TEST **(08 Hours)**

Overview of Testing methodologies, components tested & their characteristics, Challenges in testing, Types of Testers (Automated test Equipment & Benchtop Testers), Components & Subsystems of Testers, Principles of Functional Testing, Parametric/ Boundary Scan /In-Circuit Test/ Flying Probe Test, Test Data Analysis, Design for Testability & Tester Calibration & Maintenance, Future Trends

ELECTRICAL AND PHYSICAL FAILURE ANALYSIS **(05 Hours)**

Package failure modes, Failure detection mechanisms, Failure analysis tools, Test programs debugging, Data Analytics, ESD & EMI Management

SEMICONDUCTOR PACKAGE MATERIALS AND QUALIFICATION **(09 Hours)**

Reliability testing & qualification- MST/MSL, TC/TS, HAST & uHAST, Mold Compounds (Moldability), Underfill Materials, Die Attach Adhesives & Films, Substrate Technology, Bonding Wire, Solder & Dielectric materials

INDUSTRIAL QUALITY AND STATISTICAL PROCESS CONTROL **(13 Hours)**

Quality Control Plan (QCP) & Quality Management System (QMS), Incoming Material Inspection, In-Line Quality, Measurement System Analysis, Statistical analysis methods, Statistical Process Control (SPC), Fault Detection Control (FDC), Run-to-Run Control (R2R), Auto Defect Classification (ADC), Data Analytics, Machine Communication Protocol and System Integration

Total Contact Time: = 45 Hours

Course Teaching Plan (Offered by Micron Academic Alliance)

1. Micron Subject Matter Experts across the globe provide the course lectures through online zoom webinar sessions to bring semiconductor package manufacturing and test knowledge to India academia.
2. Institute faculty (course in charge) are required clear students doubts in this course.
3. Course in charge from university required to take care of arranging the online lecturer setup in classrooms, student assessment, grades and exams, attendance etc.

3. Books / Journals Recommended

1. Lau, J. H., Semiconductor Advanced packaging. Springer Nature, 2021.
2. Bar-Cohen et al., Encyclopaedia of Packaging Materials, Processes, and Mechanics. In World Scientific, 2019
3. Moyne, J., Del Castillo, E., & Hurwitz, A. M., Run-to-Run control in semiconductor manufacturing, CRC Pres, 2000
4. Emiliano R. Martins, Essentials of Semiconductor Device Physics, Wiley, 2022.
5. Harman, G., Wire Bonding in Microelectronics, 3/E. McGraw-Hill Education, 2010
6. Ardebili, H., Zhang, J., & Pecht, M. G., Encapsulation technologies for electronic applications, William Andrew, 2018
7. Chen, A., & Lo, R. H., Semiconductor packaging: Materials Interaction and Reliability, CRC Press, 2016
8. Gan, C. L., & Chen-Yu, H., Interconnect reliability in advanced memory device packaging, Springer, 2023
9. Roffel, B., & Betlem, B. H., Advanced practical process control. In Springer eBooks, 2004

M. Tech. I (VLSI & Embedded Systems) Semester – II LOW POWER VLSI DESIGN ECVL112	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the physics of power dissipation in CMOS
CO2	Estimate power that occurs due to various signal and circuit phenomena
CO3	Design low power CMOS circuits
CO4	Analyze VLSI Design Methodologies for achieving low power
CO5	Evaluate algorithms for power estimation and optimization

2. Syllabus

PHYSICS OF POWER DISSIPATION IN CMOS **(08 Hours)**

Submicron MOSFET, Gate induced drain leakage, Short circuit dissipation, Dynamic dissipation, Load capacitance, Low power limits: Hierarchy limits, fundamental limits, device limit, circuit limit, system limit

POWER ESTIMATION **(08 Hours)**

Probabilistic Techniques for Signal activity Estimation, Statistical Technique to estimate average power, Estimation of Glitch power, Power sensitivity analysis, Input vector compaction, Domino CMOS, Circuit reliability, High level power estimation, Estimation of maximum power

DESIGN OF LOW POWER CMOS CIRCUITS **(09 Hours)**

Circuit Design Styles, Leakage current and submicron device issues, Low voltage circuit design techniques, Multiple supply voltages

VLSI DESIGN METHODOLOGY FOR LOW POWER **(10 Hours)**

Low power physical design, Low power gate level design (Logic minimization, spurious transition reduction and precomputation based reduction), Low power architectural level design (parallelism, pipelining, distributed processing and power management) , Algorithmic level power reduction (switched capacitance and switching activity reduction

ALGORITHMS FOR LOW POWER **(10 Hours)**

Algorithms for power estimation (Gate level, Architectural level, Instruction level and bus switching activity), Power optimization: Algorithm transformations, minimizing memory access, Instruction selection/ordering and power management, Automated low power code generation, Codesign for Low power

Total Contact Time: = 45 Hours

3. Books Recommended

1. Kaushik Roy, Sharat C. Prasad, “Low-Power Cmos Vlsi Circuit Design”, John Wiley & Sons, 2009.
2. A. Bellamour, and M. I. Elmasri, “Low Power VLSI CMOS Circuit Design”, Springer US, 2012.
3. Anantha P. Chandrakasan and Robert W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, 2012.
4. Christian Piguet, “Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools”, Tayler and Francis (CRC), 2006.
5. Sung-Mo Kang and Y. Leblebici, “CMOS Digital Integrated Circuits”, Tata Mcgrag Hill, 3rd edition, 2003

M. Tech. I (VLSI & Embedded Systems) Semester – II VLSI ARCHITECTURES FOR DSP ECVL114	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe DSP algorithms using data flow graphs and various VLSI architectures for signal processing.
CO2	Apply fast convolution methods for optimization.
CO3	Analyze critical path algorithm and strength reduction.
CO4	Evaluate signal processing architectures based on area and power.
CO5	Design VLSI architectures for the signal processing based on specifications.

2. Syllabus

DSP CONCEPTS **(10 Hours)**

Linear system theory, DFT, FFT, DCT realization of digital filters. Typical DSP algorithms, DSP applications, Data flow graph presentation of DSP algorithm.

ARCHITECTURAL ISSUES **(13 Hours)**

Binary Adders, Binary multipliers, Multiply Accumulator (MAC) and Sum of Product (SOP). Pipelining and Parallel Processing, Retiming, Unfolding, Folding, Register Minimization Technique and Systolic architecture design, Coordic Architecture, Distributed Arithmetic Architecture

FAST CONVOLUTION **(11 Hours)**

Cook-Toom algorithm modified Cook-Toom algorithm, Winograd algorithm, modified Winograd algorithm, Algorithmic strength reduction in filters and transforms, DCT and inverse DCT, parallel FIR filters.

POWER ANALYSIS IN DSP SYSTEMS **(11 Hours)**

Scaling versus power consumption, power analysis, power reduction techniques, power estimation techniques, low power IIR filter design, Low power CMOS lattice IIR filter.

Total Contact Time: = 45 Hours

3. Books Recommended

1. Keshap K. Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, 1st Ed., John Wiley, 2007.
2. Keshab K. Parhi and Takao Nishitani, Marcel Dekker “Digital Signal Processing for Multimedia Systems”, 1st Ed., CRC Press, 1999.
3. U. Meyer-Baese, “Digital Signal processing with Field Programmable Arrays”, 3rd Ed., Springer, 2007.
4. V. K. Madisetti, “VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis”, IEEE Press, New York, 1995.
5. S. Y. Kung, H. J. Whitehouse, “VLSI and Modern Signal Processing”, 1st Ed., Prentice Hall, 1985.

M. Tech. I (VLSI & Embedded Systems) Semester – II VLSI SYSTEM DESIGN ECVL116	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe systems levels issues related to interconnect and its solution.
CO2	Apply the system decompositions in data path and control path.
CO3	Analysis of sequential logic circuit design.
CO4	Evaluate various Timing issues and its solutions.
CO5	Design systems with shared memory architecture.

2. Syllabus

INTERCONNECT (12 Hours)

The Wire, Interconnect Parameter, Electrical and Spice Wire Model, RLC Parasitic, Signal Integrity and High Speed Behavior Of Interconnects: Ringing, Cross Talk And Ground Bounce. Layout Strategies at IC And Board Level for Local and Global Signals, Power Supply Decoupling, Advance Interconnect Techniques. Clocking strategy.

SYSTEM HARDWARE DECOMPOSITION (10 Hours)

VLSI Design Flow, Mapping Algorithms into architectures, Data Path And Control Path, Register Transfer Level Description, Control Path Decomposition (Interfacing With FSM), Pitfalls of Decomposition, Critical Path and worst case timing analysis, Control Flow And Data Flow Pipelines, Communication Between Subsystems, Control Deadlocks. Concept of hierarchical system design; Data-path element: Data-path design philosophies, fast adder, multiplier, driver etc. Timing And Control Shared Memory Data Hazards And Consistency, Mutual Exclusion.

DESIGNING OF SEQUENTIAL LOGIC CIRCUIT (10 Hours)

Timing classification; Synchronous design; Self-timed circuit design; Clock Synthesis and Synchronization: Synchronizers; Arbiters; Clock Synthesis; PLLs; Clock generation; Clock distribution; Synchronous Vs Asynchronous Design, Static And Dynamic Latches And Registers, Design And Optimization Of Pipelined Stages, Timing Issues In Digital Circuits, Handling Multiple Clock Domains, Interface Between Synchronous And Asynchronous Blocks, Set-Up And Hold Time Violation, Concept Of Meta-Stability.

MEMORY SUBSYSTEM DESIGN (13 Hours)

Memory Architecture, Shared Memory Architecture, Data Hazards and Consistency, Mutual Exclusion

Total Contact Time: = 45 Hours

3. Books Recommended

1. Rabaey Jan M., Chandrakasan Anantha and Borivoje Nikolic, "Digital Integrated Circuits (Design Perspective)", 2nd Ed., Prentice Hall of India, 2016 (Reprint).
2. Neil H. E. Weste, David. Harris and Ayan Banerjee,, “CMOS VLSI Design”, 4th Ed., Pearson Education, 2019
3. Smith M. J. S., "Application Specific Integrated Circuits", 1st Ed., Addison Wesley, 1999.
4. Dally W. J. and Poulton J. W., "Digital System Engineering", 1st Ed., Cambridge University Press, 1998.
5. Hall S. H., Hall G. W. and McCall J. A., "High Speed Digital System Design", 1st Ed., John Wiley & Sons, 2000.
6. Bakoglu H. B., "Circuit Interconnect and Packaging For VLSI", 1st Ed., Addison-Wesley, 1990.
7. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test principles And Architectures Design For Testability", 1st Ed., Morgan Kaufmann Publishers, 2006.

4. Reference Books

1. Bakoglu H. B., "Circuit Interconnect and Packaging For VLSI", 1st Ed., Addison-Wesley, 1990.
2. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test principles And Architectures Design For Testability", 1st Ed., Morgan Kaufmann Publishers, 2006.

M. Tech. I (VLSI & Embedded Systems) Semester – II SOC DESIGN ECVL118	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power.
CO2	Implement both hardware and software solutions, formulate hardware/software trade-offs, and perform hardware/software co-design.
CO3	Analyze issues in system-on-chip design associated with Interconnection Structures, performance and power consumption.
CO4	Use of SystemC programming and HLS.
CO5	Design and optimize a modern System-on-a-Chip.

2. Syllabus

SOC DESIGN APPROACH **(08 Hours)**

Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores; Co-processor; Cache; DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design

HARDWARE-SOFTWARE CO-SYNTHESIS **(09 Hours)**

Partitioning, Cycle Time, Die Area-and-Cost, Power, Area-time-Power Trade-offs and Chip Reliability, Real-time scheduling, hardware acceleration

VIRTUAL PROTOTYPING AND HLS **(10 Hours)**

Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling & Electronic System-Level Languages, Hardware Accelerators, Media Instructions, Co-processors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture Techniques, Source-Level Optimizations

SOC INTERCONNECTION STRUCTURES: **(10 Hours)**

Bus-based Interconnection, Bus protocols: AMBA AXI Bus; AXI4-Stream; IBM Core Connect; Avalon, Interconnection Structures, Network on Chip - NoC Interconnection and NoC Systems, IP interfacing

PERFORMANCE / POWER ANALYSIS OF SOCS **(08 Hours)**

System-level modeling and integration, Simulation platform for performance analysis of SoC/MPSoC, Use cases and examples.

Total Contact Time: = 45 Hours

3. Books Recommended

1. Veena Chakravarthi, “A Practical Approach to VLSI System on Chip (SoC) Design-A Comprehensive Guide”, Springer, 2020
2. S. Pascricha and N. Dutt, “On-Chip Communication Architectures, System on Chip Interconnect”, Morgan Kaufmann-Elsevier Publishers, 2008,
3. Keating, M., “The Simple art of SoC design”, Springer, 2011,.
4. P. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer, 2009,
5. Ghenassia, F., “Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems”, Springer, 2010
6. Grotker, T., Liao, S., Martin, G. & Swan, S., “System design with SystemC”, Springer, 2002

M. Tech. I (VLSI & Embedded Systems) Semester – II CMOS RF IC Design ECVL120	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Select a transceiver specification appropriate for the communication link.
CO2	Demonstrate Analog and Digital Modulation for RF circuits.
CO3	Analyze the Low Noise Amplifier (LNA).
CO4	Evaluate the appropriate mixers and oscillators for the desired applications.
CO5	Design of PLL using appropriate loop filter, phase detector and frequency synthesizer.

2. Syllabus

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: (08 Hours)

Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion, S-parameters with Smith chart, Passive IC components.

POWER AMPLIFIERS AND MATCHING NETWORKS (06 Hours)

Class A, AB, B and C Power amplifiers, modulation and characteristics of power amplifiers, Design examples. Impedance transformations and matching; L-matches, Pi- & T-matches, tapped-capacitor match.

LOW NOISE AMPLIFIERS (12 Hours)

LNA Topologies: Common-Source Stage with Resistive Feedback, Common Gate, Cascode CS Stage with Inductive Degeneration, Variants of Common-Gate LNA, Noise-Cancelling LNAs, Reactance-Cancelling LNAs Gain Switching, Band Switching, Differential LNAs, Nonlinearity Calculation

MIXERS AND OSCILLATORS (11 Hours)

Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators

PLL AND FREQUENCY SYNTHESIZERS (08 Hours)

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters, Some discussion on available CAD tools for RF VLSI design

Total Contact Time: = 45 Hours

3. Books Recommended

1. T. H. Lee, “The Design of CMOS RF Integrated Circuits”, Cambridge, 2012.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2013.
3. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.
4. C.C. Enz and E.A. Vittoz, Charge-based MOS transistor Modelling The EKV Model for Low-Power and RF IC Design By, Wiley, 2006
5. Christopher Bowick, “RF Circuit Design”, Newnes, 2007

M. Tech. I (VLSI & Embedded Systems) Semester – II NANOSCALE DEVICES ECVL122	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the MOS Device Engineering nanoscale
CO2	Describe and illustrate Non Classical MOS Device Structures
CO3	Analyze Emerging Nanoscale Devices and its property
CO4	Evaluate the Ballistic theory of carrier transport and Model the characteristics the nanoscale MOS Devices
CO5	Design the Nanoscale Memory and different emerging memory devices.

2. Syllabus

MOS DEVICE ENGINEERING **(07 Hours)**

CMOS Scaling, Channel, and Source Drain Engineering. Gate Oxide Scaling and Reliability, High K Dielectrics, Metal Gate Transistor, Effect of non-idealities in CV characteristics, Subthreshold slope engineering.

NON-CLASSICAL TRANSISTORS **(11 Hours)**

Silicon on Insulator (SOI) MOSFETs, Partially Depleted (PD) SOI MOSFETs, Fully Depleted (FD) SOI MOSFETs, Ultrathin Body (UTB) SOI, Fin FET, Surround Gate FET, Germanium Based MOSFETs, Schottky Barrier S/D MOSFETs, Strained Layer High Mobility MOSFETS, GaAs FETs,HEMTS: Modulation (delta) Doping, Analysis of III-V Heterojunctions, Charge Control, I-V characteristics, HBTs: Structure, Basic Operation, Technological Aspects, I-V characteristics

EMERGING MOS DEVICES **(10 Hours)**

Junctionless MOSFET, Tunnel FETs, Negative Capacitance FETS.Beyond Silicon Technology: Organic FETs, 2D-Materials Based FETs: CNT, Nanowire, MOS2, MOSe2, Black Phosphorus, and current trends.

MODELLING OF NANOSCALE MOSFETS **(10 Hours)**

Ballistics Transport, NEGF Formalism, Physical view of the nanoscale MOSFETs, Natori's theory of the ballistic MOSFET, Nondegenerate, degenerate, and general carrier statistics The ballistic MOSFET, Quantum Transport in Nanoscale MOSFETs, Role of the quantum capacitance, Scattering Theory of the MOSFETs

NANOSCALE MEMORY DEVICES **(07 Hours)**

Emerging memory technologies: Phase Change Memory (PCM); Resistive Random-Access Memory; Magnetoresistive Random Access Memory (MRAM); Ferroelectric Random-Access Memory (FeRAM); MOTT Memory, Comparison and future directions.

Total Contact Time: = 45 Hours

3. Books Recommended

1. Taur and Ning, “Fundamentals of Modern VLSI Devices” Cambridge University Press, 2009.
2. M. S Lundstrom and J. Guo,“Nanoscale Transistors: Device Physics, Modeling and Simulation” Springer, 2006
3. D Esseni P Palestri and L Selmi,“Nanoscale MOS Transistors: Semi-Classical Transport and Applications”, Cambridge University Press, 2011.
4. Tseung-Yuen Tseng and Simon M. Sze, “Nonvolatile memories-Materials, Devices and Applications”, American Scientific Publishers, 2012
5. Simone Raoux and Matthias Wuttig, “Phase change materials-Science and Applications”, Springer 2009

M. Tech. I (VLSI & Embedded Systems) Semester – II SEMICONDUCTOR PACKAGING ECVL124	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the traditional packaging technologies and the process involved
CO2	Demonstrate various advanced packaging materials, substrates, technologies, interconnects, and thermal management.
CO3	Analyze the reliability of advanced packaging technologies
CO4	Evaluation of emerging technologies in the field of packaging.
CO5	Design of Semiconductor Packaging

2. Syllabus

INTRODUCTION TO SEMICONDUCTOR PACKAGING (09 Hours)

Definition of packaging and its significance in various industries; Introduction to packaging and its importance in Modern Electronics.
Traditional packaging technologies: Leaded and leadless packages, surface mount technology (SMT), and ball grid array (BGA).

ADVANCED PACKAGING (12 Hours)

Introduction to advanced packaging: Advanced packaging and its importance in evolving technology requirements. Benefits and challenges of advanced packaging. Advanced packaging integrated technology: 2.5D and 3D packaging, Optoelectronics packaging, MEMS and Sensors packaging, Memory packaging.
Advanced packaging interconnects: Interconnect technologies in advanced packaging: flip chip bumping, solder balls, and through-silicon vias (TSVs).

ADVANCED PACKAGING MATERIALS AND SUBSTRATES (08 Hours)

Substrates and materials used in advanced packaging, such as organic substrates, build-up substrates, redistribution layers (RDLs), interposers, and fan-out substrates. Substrates and materials: properties, fabrication techniques, and performance characteristics.

THERMAL MANAGEMENT IN ADVANCED PACKAGING (05 Hours)

Importance of thermal management in advanced packaging.
Thermal management techniques: heat sinks, thermal interface materials (TIMs), and thermal vias.

TESTING AND RELIABILITY IN ADVANCED PACKAGING (06 Hours)

The testing methodologies and reliability considerations specific to advanced packaging. Package-level testing, interconnect testing, and reliability testing. Failure analysis techniques and strategies for package reliability.

FUTURE TRENDS AND EMERGING TECHNOLOGIES (05 Hours)

Emerging trends in advanced packaging and their potential impact. Future developments and opportunities in the field.

Total Contact Time: = 45 Hours

3. Books Recommended

1. Fundamentals of Device and Systems Packaging Technologies and Applications by Rao R. Tummala, McGraw-Hill Publications, Second Edition, 2019.
2. Microelectronics Packaging Handbook by Rao R. Tummala, Eugene J. Rymaszewski, and Alan G. Klopfenstein, Springer, 1997.
3. Semiconductor Advanced Packaging by John. H. Lau, Springer, 2021
4. Semiconductor Packaging: Materials Interaction and Reliability, Chen, Andrea, Lo, Randy Hsiao-Yu, CRC Press, 2011.
5. 3D IC Integration and Packaging 1st Edition by John H. Lau, McGraw Hill, 2015.

Additional Resources:

1. Relevant Journal and Conference publications.

M. Tech. I (VLSI & Embedded Systems) Semester – II NEUROMORPHIC COMPUTING ECVL126	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the fundamentals of Neuro Science
CO2	Use the concepts of Neuroscience for neuromorphic design
CO3	Analyze principles of spiking neural networks
CO4	Apply neuromorphic engineering for real-life problems
CO5	Design spiking neural networks using various approaches

2. Syllabus

FUNDAMENTALS OF NEURO SCIENCE (09 Hours)

Introduction to Neuromorphic Engineering; Signaling and operation of biological neurons, neuron models, signal encoding and statistics; Synapses and plasticity rules, biological neural circuits;

NEUROMORPHIC DESIGN PRINCIPLES (10 Hours)

FETs - device physics and sub-threshold circuits; Analog and digital electronic neuron design; Non-volatile memristive semiconductor devices; Electronic synapse design;

OPERATIONAL PRINCIPLES AND LEARNING IN SPIKING NEURAL NETWORKS (09 Hours)

Spiking Neural Networks, Learning in Shallow SNNs, Learning in Deep SNNs, Learning Through Modulating Weight-Dependent STDP in Multilayer Neural Networks, Simulation Results,

HARDWARE IMPLEMENTATIONS OF SPIKING NEURAL NETWORKS (10 Hours)

The Need for Specialized Hardware, Digital SNNs: Large-Scale SNN ASICs; Small/Moderate-Scale Digital SNNs; Hardware-Friendly Reinforcement Learning in SNNs; Hardware-Friendly Supervised Learning in Multilayer SNNs, Analog/Mixed-Signal SNNs: Basic Building Blocks; Large-Scale Analog/Mixed-Signal CMOS SNNs; Other Analog/Mixed-Signal CMOS SNN ASICs; SNNs Based on Emerging Nanotechnologies; Case Study: Memristor Crossbar Based Learning in SNNs

ADVANCES IN NEUROMORPHIC COMPUTING (07 Hours)

Brain-Inspired Neuromorphic computing, Neuromorphic Hearing, Neuromorphic Vision

Total Contact Time: = 45 Hours

3. Books Recommended

1. Dale Purves, “Neuroscience”, Sinauer, 3rd Ed., 2011,
2. Carver Mead, “Analog VLSI and Neural Systems”, Addison-Wesley, 1989,
3. Nan Zheng, Pinaki Mazumder, “Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design”, Wiley, 2019
4. Richard F. Lyon, Tor Sverre Lande, “Neuromorphic Systems Engineering: Neural Networks in Silicon”, Springer US, 1998
5. Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, “Principles of neural science”, McGraw Hill 2012,
6. Khaled Salah Mohamed, “Neuromorphic Computing and Beyond”, Springer International Publishing, 2020
7. Steve Furber (ed.), Petrut Bogdan (ed.), "SpiNNaker: A Spiking Neural Network Architecture", Boston-Delft: now publishers, 2020

M. Tech. I (VLSI & Embedded Systems) Semester – II MIXED SIGNAL IC DESIGN ECVL128	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand sample and hold circuits based on CMOS and BiCMOS. Compare and contrast various S/H circuits.
CO2	Apply advanced techniques for bandgap references, comparators, current mirrors and operational amplifiers.
CO3	Evaluate concepts of Oversampled ADCs, Noise shaping and decimation filtering. Propose and design sigma-delta architecture based on specification
CO4	Analyze a variety of data converters. Compare architectures based on various metrics.
CO5	Design of various mixed signal blocks

2. Syllabus

SAMPLE AND HOLD CIRCUITS **(8 Hours)**

Sample & hold and trans-linear circuits - performance and testing of sample and hold circuits, examples of CMOS S/H circuits, bipolar and BiCMOS S/H circuits, trans-linear gain cell and multipliers. Switched capacitor circuits – op-amps, capacitors, switches, non-overlapping clocks

SWITCHED CAPACITOR CIRCUITS **(6 Hours)**

Basic operation and analysis of switched capacitor circuits, resistor equivalence of a switched capacitor, noise in switched-capacitor circuits. Comparators - specifications, op-amp as a comparator, latched comparators, examples of CMOS comparators

A TO D AND D TO A CONVERTERS **(12 Hours)**

Data convertors - ideal D/A and A/D convertors, quantization noise, accuracy and linearity. Nyquist rate DAC - Decoder-based converter, Binary-scaled converters, Thermometer-code converters, Hybrid converters. Nyquist rate ADC - Successive-approximation converters, Algorithmic (or cyclic) A/D Converter, Pipelined A/D converters, Two-step A/D converters, Interpolating A/D converters, folding A/D converters, time-interleaved A/D converters

OVERSAMPLED DATA CONVERTERS **(12 Hours)**

Oversampling ADCs - Oversampling without noise shaping - quantization noise modeling, white noise assumption, • oversampling advantage, the advantage of 1-bit D/A converters. Oversampling with noise shaping - noise-shaped delta-sigma modulator, first-order noise shaping, switched-capacitor realization of a first-order A/D converter, quantization noise power of 1-bit modulators. System architectures, Digital decimation filters, Multi-bit oversampling converters

MIXED SIGNAL SUBCIRCUITS **(7 Hours)**

Linearized PLL models, Design of PLL's and DLL's and frequency synthesizers, VCO, Jitter and phase noise, Electronic oscillators

Total Contact Time: = 45 Hours

3. Books Recommended

1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, 2nd Edition, John Wiely & Sons, 2012.
2. B. Razavi, “Principles of Data Conversion System Design”, 1st Edition, Wiley-IEEE Press, 1994
3. R. J. Baker, “CMOS Mixed Signal circuit Design”, 2nd Edition, Wiley 2008
4. M.Gustavsson, J. J. Wikner, and N. N. Tan, "CMOS Data Conversion for Communications", Kluwer 2000.
5. Emad N. Farad and Mohamed I. Elmasry, “Mixed Signal VLSI Wireless Design: Circuits and Systems”, Kluwer 2002

M. Tech. I (VLSI & Embedded Systems) Semester – II MEMORY TECHNOLOGY ECVL130	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand fundamental concepts of different memory technologies
CO2	Implement of static RAM & dynamic RAM
CO3	Compare the various memory technologies
CO4	Evaluate the various memory technologies
CO5	Design different advanced memory technologies

2. Syllabus

INTRODUCTION TO MEMORY TECHNOLOGIES **(08 Hours)**

Memory organization and overview of memory technology: market, trends and technologies, Overview of volatile and non-volatile memory technology, Static Random-Access Memory (SRAM), Dynamic RAM (DRAM), 1T-1C architecture, Capacitor-less DRAM, On-chip memory, on-chip memory types.

STATIC RAM **(10 Hours)**

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

DYNAMIC RAM **(9 Hours)**

DRAMs, MOS DRAM Cell, Bi-CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

FLASH MEMORY **(8 Hours)**

Flash memory: NOR and NAND architecture, Poole Frenkel emission and Fowler-Nordheim tunneling, floating gate (FG) and charge-trap (CT) NAND flash, reliability, scaling and multi-bit capability (MLC) 3D NAND, BICS, TCAT, V-NAND, VG NAND Flash, reliability and MLC

ADVANCED MEMORY TECHNOLOGIES **(10 Hours)**

High-density Memory Packing Technologies, Emerging non-volatile memories (eNVM): Resistive RAM (RRAM), unipolar and bipolar stacks, oxygen vacancy and ionic transport, reliability and endurance, Phase change memory (PCM), Ferroelectric RAM (FeRAM), Gallium Arsenide (GaAs) FRAMs, Conductive Bridge RAM (CBRAM) and Spin-transfer Torque Magnetic RAM (STT-MRAM)

Total Contact Time: = 45 Hours

3. Books Recommended

1. S. Yu, “Semiconductor Memory Devices and Circuits”, 1st Edition, CRC Press, 2022.
2. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing, and Reliability”, 1st Edition, Wiley IEEE, 2013
3. Kiyoo Itoh, “VLSI Memory Chip Design”, 1st Edition, Springer, 2001
4. N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd Edition. Pearson, 2006
5. Y. Nishi and Magyari-Kope, “Advances in non-volatile memory and storage technology”, Woodhead Publishing, 1st Edition, 2019.
6. Keeth, Baker, Johnson, and Lin, “DRAM Circuit Design: Fundamental and High-Speed Topics”, 2nd Edition, Wiley, IEEE 2007.

M. Tech. I (VLSI & Embedded Systems) Semester – II HIGH-SPEED INTERCONNECT ECVL132	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the VLSI interconnect, parasitic components and interconnect technology
CO2	Analyze interconnect delay
CO3	Evaluate crosstalk
CO4	Design PLL/DLL and Clock and data recovery (CDR) / deserializers
CO5	Design Equalization and equalizers and serializers

2. Syllabus

VLSI INTERCONNECTS **(05 Hours)**

Interconnections for VLSI Applications-Copper Interconnections- Method of Images- Method of Moments- Even and Odd Mode Capacitances- transmission line equations- miller's theorem-Resistive interconnects as ladder network-Propagation modes in micro strip interconnects-slow wave propagations-Propagation delay

PARASITIC COMPONENTS **(05 Hours)**

Parasitic resistances, capacitances and inductances- approximate formulas for capacitances-Green's function method using Images and Fourier integral approach- network Analog method-Interconnection Capacitances and Inductances on Silicon and GaAs Substrates-Inductance extraction and copper interconnections for resistance modeling.

INTERCONNECTION DELAYS **(05 Hours)**

Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections, parallel multilevel interconnections and crossing interconnections- parallel interconnection models for micro strip line- modeling of lossy parallel and crossing interconnects- high frequency losses in micro strip line- Expressions for interconnection delays-Active interconnects.

CROSS TALK ANALYSIS **(06 Hours)**

Lumped capacitance approximation- coupled multi conductor MIS micro strip line model for single level interconnects- frequency domain level for single level interconnects- transmission line level analysis of parallel multilevel interconnections-Analysis of Crossing Interconnections-Compact Expressions for Crosstalk Analysis- Multi conductor Buses in GaAs High-Speed Logic Circuits.

Phase-locked loops (PLLs) and delay locked loops (DLLs) **(06 Hours)**

Basic Building blocks,pf PLL/DLL, Loop analysis, A brief overview of non-idealities in the PLLs/DLLs, Jitter and phase noise (and relationship between them), Jitter transfer functions in DLLs and PLLs, BER estimation based on jitter,

Clock and data recovery (CDR) / deserializers **(06 Hours)**

Phase detectors (linear/non-linear, full-rate/nth-rate etc. and some examples, Basic circuit level blocks: Latches, flip-flops, XOR gates, muxes etc. in Current Mode Logic (CML), Circuit level bandwidth enhancement techniques, Tunable delays using tunable delay cells and phase interpolators, Voltage controlled oscillators (VCOs), Multi-phase clock generation. g) CDR architectures

Equalization and equalizers and serializers **(06 Hours)**

Channel model and inter-symbol-interference (ISI), Pre-cursor and post-cursor ISI, Analog domain equalizers i. CTLE (continuous time linear equalizers). ii. FFE (feed-forward equalizers). iii. Non-linear equalizers (decision-feedback equalizers), Equalization in the digital domain, Equalizer training and blind equalization techniques, Eye monitor circuits for equalizers.
Transmitters and serializers: Block diagram of a serializer, LVDS (low-voltage differential signaling) and impedance matching, Pre-emphasis (FIR) equalization for transmitters

INTERCONNECTION TECHNOLOGIES **(06 Hours)**

Transmission Line Models of Lossy Waveguide Interconnections- Optical interconnects - Superconducting Interconnections- Nanotechnology Circuit Interconnections (Graphene and CNT) - Potential Technologies- Nanotube Integrated Circuits.

Total Contact Time: = 45 Hours

3. Books Recommended

1. Ashok K. Goel “High-Speed VLSI Interconnections”, 2nd Edition, Wiley-IEEE Press, August 2007.
2. S. H. Hall and H.L. Heck , Advanced Signal Integrity for High-Speed Digital Designs, John Wiley & Sons, 2009.
3. Behzad Razavi, Design of Integrated Circuit for Optical Communications, McGraw-Hill, 2003.
4. H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI” Massachusetts: Addison-Wesley Publishing Company, 2000.
5. Hall, S.H., G. W. Hall and J. McCall, “High-Speed Digital System Design”, First Edition. Wiley-Interscience, 2000.

M. Tech. I (VLSI & Embedded Systems) Semester – II IMAGE PROCESSING & COMPUTER VISION ECCS102	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Understand the basic of image formation and use of different image transforms with their properties.
CO2	Apply techniques for image enhancement both in spatial and frequency domains
CO3	Analyze causes for image degradation and apply restoration techniques.
CO4	Evaluate different image segmentation techniques and develop solutions using Mathematical morphology concept.
CO5	Develop the image compression techniques in spatial and frequency domains

2. Syllabus

IMAGE PROCESSING SYSTEM **(04 Hours)**

Camera Model, Image Representation, Image Sampling, Quantization, Resolution, Human Visual System, Classification of Digital Images, Image Types, Elements of an Image-processing System, Image File Formats, Relationships Between Pixels-Nearest Neighbor, Adjacency, Connectivity, Regions, and Boundaries; Distance Measures.

IMAGE ENHANCEMENT & IMAGE TRANSFORMS **(10 Hours)**

Image Enhancement in spatial domain, Enhancement through Point Operation, Histogram Manipulation, Gray-level Transformation, Neighborhood Operation, filtering operation in spatial domain, Bit-plane Slicing, Enhancement in the Frequency Domain,2D Convolution, 2D Discrete Fourier Transform, Homomorphic Filter, Zooming Operation,

IMAGE RESTORATION/DENOISING AND IMAGE REPRESENTATION & DESCRIPTION **(10 Hours)**

Linear, Position-Invariant Degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering Classification of Noise in Image, Median Filtering, Trimmed Average Filter, Adaptive filters, Performance Metrics in Image Restoration, Applications of Digital Image Restoration. Image Image Compression Fundamentals, study of Image representation and description techniques.

IMAGE SEGMENTATION AND MATHEMATICAL MORPHOLOGY **(06 Hours)**

Point, Line, and Edge Detection, Thresholding, Region-Based Segmentation, Basic Morphological Operations-Opening, Closing Operators, Dilation and Erosion, Morphological Algorithms, Applications.

IMAGE FORMATION **(05 Hours)**

Pinhole and Perspective Projection, Image Magnification, Vanishing Point, Image Formation using Lenses, Gaussian Lens Law, Focal Length, Two Lens System, Aperture of the Lens, Lens Defocus, Blur Circle, Depth of Field, Lens Related Issues.

RECONSTRUCTION **(10 Hours)**

Light Flux, Radiant Intensity, Surface Irradiance, Scene Radiance, BRDF, Reflectance Models, Surface Orientation, Reflectance Map, Photometric Stereo, Shape from Shading, Depth from Focus, Depth from Defocus.

Total Contact Time: = 45 Hours

3. Books Recommended

1. R. C. Gonzalez, R. E. Woods, Digital Image Processing, Pearson Education. 3rd Ed.,2016
2. Jain A.K., Fundamentals of Digital Image Processing, Prentice-Hall, 2002.
3. Sonka M. Hlavac V., Boyle R., "Image Processing, Analysis and Machine Vision", Cengage Learning, 2nd Ed. Indian Reprint, 2009
4. Manas Kamal Bhuyan, “Computer Vision and Image Processing Fundamentals and Applications”, Taylor & Francis, CRC Press, 2020.
5. Pratt W.K., Digital Image Processing, John Wiley, IV Edition, 2007.
6. Berthold Horn, Robot vision, MIT press, 1986.
7. Richard Hartley, Andrew Zisserman, Multiple view geometry in computer vision, Cambridge university press, 2003.

M. Tech. I (VLSI & Embedded Systems) Semester – II WIRELESS COMMUNICATION ECCS104	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe the basic concepts and terminology of Communication and wireless communication
CO2	Classify the channel models, modulation schemes like spread spectrum and multicarrier modulation
CO3	Demonstrate the concept of Spread Spectrum Technology and multicarrier modulation scheme to develop a secured wireless communication link
CO4	Analyze the various channel models and modulation schemes from the perspective of wireless channel performance.
CO5	Evaluate the advanced wireless communication challenges and solutions in terms of advanced techniques

2. Syllabus

GENERAL CONSIDERATIONS **(10 Hours)**

General considerations about radio waves over wireless channel, Radio wave propagation and the atmosphere, basic propagation mechanisms, classification of fading channels, large scale fading, shadowing, small-scale fading and multipath, statistics of fading coefficient, BER of wired and wireless communication system, diversity, power profile, delay spread, coherence bandwidth, Doppler, Doppler spectrum.

SPREAD SPECTRUM MODULATION **(12 Hours)**

Basic principle of Orthogonality, spreading code, CDMA, generation and properties of PN sequence, random spreading sequence and their properties, advantages of CDMA, rake receiver, performance analysis of CDMA downlink and uplink scenarios, near far problem in CDMA

MULTI-CARRIER MODULATION AND OFDM **(13 Hours)**

Introduction to Multicarrier modulation, multicarrier transmission and reception scheme, bottleneck in multi-carrier modulation scheme, introduction to OFDM, OFDM transmission and reception schemes, cyclic prefix, carrier frequency offset in OFDM, PAPR in OFDM, SC-FDMA.

MIMO **(10 Hours)**

Introduction spatial multiplexing, MIMO system model, zero forcing receiver, MIMO-MMSE receiver, SVD based optimal MIMO transmission and reception, optimal power allocation in MIMO, space time coding, Non-linear MIMO receiver-V-BLAST, MIMO beam forming, MIMO-OFDM

Total Contact Time: = 45 Hours

3. Books Recommended

1. T. S. Rappaport, “Wireless Communications: Principles and Practice”, Pearson Education, 2nd Edition, 2010.
2. Molisch Andreas F, “Wireless Communications”, Wiley, 2nd Edition, 2011.
3. Goldsmith Andrea, “Wireless Communications”, Cambridge University Press,2002.
4. Yong Soo Cho, Jaekwon Kim, Won Young Yang, and Chung G. Kang, "MIMO-OFDM Wireless Communications with MATLAB" Wiley, 1st Edition, 2010.
5. Upena Dalal, “Wireless Communication”, Oxford University Press, 1st Edition, 2008.

M. Tech. I (VLSI & Embedded Systems) Semester – II MICROWAVE INTEGRATED CIRCUITS ECCS116	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Describe the Microstrip lines, slot lines, co-planar line, and Microwave and millimeter wave circuit.
CO2	Implement the models for passive components, active device and impedance matching network.
CO3	Analyze the design and stability of microwave integrated circuits, Substrate Integrated Waveguide, Metamaterial-Based Compact Microwave and Millimetre Wave Circuit.
CO4	Evaluate the parameter of passive microwave components, active device and impedance matching network.
CO5	Develop an ability to evaluate the performance of microwave integrated circuits by using different measurements and testing techniques.

2. Syllabus

INTRODUCTION TO MICROWAVE INTEGRATED CIRCUITS (03 Hours)

Introduction to Monolithic Microwave Integrated Circuits (MMICs), their advantages over discrete circuits, MMIC fabrication techniques, Thick and Thin film technologies and materials, encapsulation and mounting of active devices, Microstrips on semiconductor substrates.

MICRO-STRIP LINES (03 Hours)

Planar transmission lines for MICs. Method of Conformal transformation for microstrip analysis, concept of effective dielectric constant, Effective dielectric constant for microstrip, Losses in Microstrip

SLOT LINES (04 Hours)

Slot Line Approximate analysis and field distribution, Transverse resonance method and evaluation of slot line impedance, comparison with Microstrip line.

FINE LINES AND COPLANAR LINES (03 Hours)

Fin lines & Coplanar Lines. Introduction, Analysis of Fin lines by Transverse Resonance Method, Conductor loss in Fin lines. Introduction to coplanar wave guide and coplanar strips.

LUMPED ELEMENTS FOR MICS (04 Hours)

Use of Lumped Elements, Capacitive elements, Inductive elements and Resistive elements

MATCHING AND BIASING NETWORKS (03 Hours)

Impedance Matching using Discrete Components, Microstrip Line Matching Networks

FUNDAMENTALSOF CMOS TRANSISTORS FOR RFIC DESIGN (04 Hours)

MOSFET Basics, MOSFET Models, Fundamentals of Stability, Determination of Stable and Unstable Regions, Stability Consideration for N-Port Circuits, Noise Figure Circles, Constant VSWR Circles. Broadband, High Power and Multistage Amplifiers, Low Noise Amplifier Design.

MICROWAVE IC DESIGN AND MEASUREMENT TECHNIQUES (03 Hours)

MIC Measurement, Testing and Applications: MIC measurement system, measurement techniques – S parameter measurement, noise measurement, MIC applications.

SUBSTRATE INTEGRATED CIRCUITS (08 Hours)

Substrate Integrated Waveguide, Substrate Integrated Image Guide, Substrate Integrated Non-radiative Dielectric Guide, Substrate Integrated Feeding Network, Substrate Integrated Divider, Substrate Integrated Phase Shifter, Substrate Integrated Coupler, Substrate Integrated Circuit–Related Transition.

METAMATERIAL-BASED COMPACT MICROWAVE AND MILLIMETRE WAVE CIRCUIT DESIGN (10 Hours)

Designs of True-Time-Delay Lines and Phase Shifters based on CRLH TL Unit Cells, Perfect Metamaterial Absorbers in Microwave and Terahertz Bands, Metamaterial-Based Compact Filter Design, Magnetically Tunable Unidirectional Electromagnetic Devices Based on Magnetic Surface Plasmon, Compact Coplanar Waveguide Metamaterial-Inspired Lines and its use in Highly Selective and Tunable Bandpass Filters.

(Total Contact Hours: 45)

3. Books Recommended

1. K.C. Gupta, “Microwave Integrated Circuits”, 1st Ed., Wiley eastern Pvt. Ltd., 1975.
2. Inder Bahl; Maurizio Bozzi; Ramesh Garg, Microstrip Lines and Slotlines, 3rd Ed., Artech, 2013.
3. T. H. Lee, “The Design of CMOS radio Frequency Integrated Circuits”, 2nd Ed., Cambridge, 2004.
4. Xun-Ya Jiang, “Metamaterials” 1st Ed., Intech, 2012.
5. Yu Jian Cheng, “Substrate Integrated Antennas and Arrays”, 1st Ed., CRC Press, 2016.

4. Reference Books

1. Bharathi Bhat, Shiban Koul, “Stripline-like transmission Lines for Microwave Integrated Ciruits”, 1st Ed., New Age International (P) Ltd. Publishers, 2007
2. Ricardo Marques, Ferran Martin, Mario Sorolla, “Materials with Negative Parameters”, 1st Ed., Wiley Interscience, 2001.
3. David M. Pozar, “Microwave Engineering”, 4th Ed., John Wiley & Sons, 2011.

M. Tech. I (VLSI & Embedded Systems) Semester – II SPEECH PROCESSING AND APPLICATIONS ECCS130	Scheme	L	T	P	Credit
		3	0	0	03

1.	Course Outcomes (COs): At the end of the course, the students will be able to
CO1	Define the fundamentals of speech processing.
CO2	Describe the different parameters of speech signal.
CO3	Apply different algorithm to extract different speech parameters.
CO4	Analyze different speech processing algorithm.
CO5	Design a speech based system for different applications.

2. Syllabus

INTRODUCTION (05 Hours)

Speech processing applications, Stationary and non-stationary signal, Stationary and non-stationary analysis of speech signal, Representation of speech signal.

SPEECH FUNDAMENTAL (06 Hours)

Basic concepts: speech production and speech perception, Speech production model, Articulatory phonetics and speech sounds, Pitch frequency and Formant frequency, Speech segmentation: voiced, unvoiced and silence, vowel, semi-vowel, consonants, diphthongs, nasal etc.

TIME DOMAIN ANALYSIS OF SPEECH SIGNAL (06 Hours)

Short-term processing of speech signal, Window function, Time domain analysis, Short-time energy, Short-time autocorrelation, Short-time zero crossing, Pitch estimation, Speech vs silence classification based on short-time energy and zero crossing rate.

FREQUENCY DOMAIN ANALSIS OF SPEECH SIGNAL (06 Hours)

Discrete Fourier Transform, Short-term Fourier transform (STFT), Filter-bank analysis, Spectrogram analysis, Cepstrum analysis, Pitch and formant estimation

LINEAR PREDICTION ANALYSIS (10 Hours)

Prediction, Linear prediction, Prediction model: All pole model and Pole zero model; Autocorrelation and covariance method; Levinson-Durbin algorithm; Inverse filtering; LP residual; Pitch frequency and formant frequency analysis using LP analysis.

SPEECH PATHOLOGY DETECTION (06 Hours)

Feature investigation, Feature extraction: Mel frequency cepstral coefficient (MFCC) and Linear prediction coefficient (LPC), Nonlinear features, Modelling (training/classification) based on machine learning and deep learning

SPEECH EMOTION CLASSIFICATION **(06 Hours)**

Effect of emotional state on speech signal, Pitch and formant analysis for different emotions, Significance of databases: acted, evoked and natural, Emotion impacted feature extraction, feature selection, Machine learning and deep learning based emotion classification.

Total Contact Time: = 45 Hours

3. Books Recommended

1. L. R. Rabiner and R. W. Schafer, “Digital Processing of Speech Signals”, 1st Ed., PearsonEducation India, 2003.
2. J. Benetsy, M. M. Sondhi and Y. Huang, “Springer Handbook of Speech Processing”, 1st Ed., Springer Verlag, 2008.
3. J. R. Deller, Jr., J. H. L. Hansen and J. G. Proakis “Discrete-Time Processing of Speech Signals”, Wiley- IEEE Press, IEEE Edition, NY, USA, 1999.
4. D. O’Shaughnessy, “Speech Communications: Human and Machine”, 2nd Ed., University Press, 2005.
5. Thomas F Quatieri, “Discrete-Time Speech Signal Processing – Principles and Practice”, 1st Ed., Pearson Education, 2006.
6. Gold, B., Morgan, N., & Ellis, D., “Speech and audio signal processing: processing and perception of speech and music” John Wiley & Sons, 2nd ED., 2011.

M. Tech. I (VLSI & Embedded Systems) Semester – II VLSI LAB – II ECVL106	Scheme	L	T	P	Credit
		0	0	6	03

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Understand of Analog VLSI Circuits, VLSI Systems and Real-time systems through simulations
CO2	Implementation of various modules and sub modules of Analog VLSI Circuits, VLSI Systems and Real-time system
CO3	Analysis the of Analog VLSI Circuits, VLSI Systems and Real-time system
CO4	Evaluate the performance of Analog VLSI Circuits, VLSI Systems and Real-time system
CO5	Design of Analog VLSI Circuits, VLSI Systems and Real-time system for the given parameters

Analog VLSI Design

Following experiments are to be performed but not limited to:

1 Obtain various V-I characteristics of PMOS and NMOS transistor.

2 Design and simulate single stage CS amplifier with different load

3 Design and simulate single stage CG and CD amplifier with different load

4 Design & Simulate following current mirrors topologies.

5 Simulate and evaluate CS amplifier with feedback.

6 Design and Simulate Cascode amplifier with following specifications:

7 Characterize and evaluate Differential amplifier with resistive load.

8 Realize 3-bit Charge Scaling DAC and find output voltage for all input combinations.

9 Design 4-bit R-2R ladder DAC using active and passive switches

10 Design and Simulate Differential amplifier with current mirror load for given specifications.

11 Design of uncompensated single stage telescopic op-amp.

12 Realize and evaluate folded cascade op-amp

VLSI System Design:

1. Introduction of IP Integrator. Implement the trigonometric function using CORDIC IP
2. Design and Simulate following using IP
   a) Single MAC , b) Parallel MAC, c) Serial MAC
3. Design and Implement Low Pass FIR filter
4. Debugging MAC unit in hardware using ILA core and viewing ILA probe data in the waveform viewer.

5. RTL 2 GDSII (Standard Cell based Semi custom ASIC Flow)

   - To study Logic synthesis:
     Using standard cell library and analysis of area, power, delay report. To obtain the design constraint file, LEC (Logic Equivalence Check), DFT (Design For Testability) insertion to verify the chip after fabrication, Gate-level netlist generation

   - To study Place and Route (PnR):
     To place all the standard cells, Macros and I/O pads with minimal area, with minimal delay and Route based on Gate-level netlist, Floor Plan, Power Plan, Placement, CTS (Clock Tree Synthesis), and Routing , DRC (Design Rule Check) error, GDS-II file generation

   - Signoff or Tapout : To fix the timing violations by post route simulation and a final layout file free from all the violations is streamed out in GDSII format

6. **Topics for Mini Projects:**
   Radix-4 Booth Multiplier, Parallel prefix adders, UART Hardware, I2C transceiver hardware, Divider, Square Root, CORDIC arithmetic, Control unit design for CPU Data path

Real Time System:

1	Write a code to create 5 threads with the pthread_create() routine.
2	Write a code to pass a simple integer to each thread.
3	Write a code to measure the time taken by each thread.
4	Write a code to set up/pass multiple arguments via a structure.
5	Write a program has different amplitudes at different carrier frequencies and phases.
6	Write a code to measure the time taken by each thread using sleep and without using sleep
7	Write a program that involves a reader and a writer thread with the help of mutex and semaphore.
8	Write a program to make an authentication system by using mutex and semaphore.
9	Calculate the different amplitudes at different digital values .
10	Write a program for blinking RGB LEDs by putting delay in between.
11	Write a program to print hello world by using a task.
12	Write a program to print hello world by five different tasks.
13	Write a program to print blinking of LEDs by using a task.
14	Write a program to implement DAC by using different tasks.

M. Tech. I (VLSI & Embedded Systems) Semester – II Mini Project ECVL108	Scheme	L	T	P	Credit
		0	0	4	02

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Explain the plan of action prototype system that addresses a specific problem or requirement within the domain of VLSI & Embedded System
CO2	Understand and modify design (for existing product) including all aspects of products , material, process, resources and standards etc.
CO3	Analyse and validate software and hardware selection
CO4	Evaluate effectiveness of practicality with respect to industry level implementation of the prototype system involving system design aspect
CO5	Design prototype with experimental result, future scalability considerations of the developed prototype and Implement final working model/software.

M. Tech. II (VLSI & Embedded Systems) Semester – III DISSERTATION PHASE - I ECVL201	Scheme	L	T	P	Credit
		0	0	28	14

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Identify any latest topic of interest from the real-world technical problems to develop a thought process for design solution with basic understanding.
CO2	Extract a detailed literature survey related to the given problem and Apply the concepts for the solution to the given problem in terms of specification, design, component selection etc.
CO3	Synthesize or Implement the model/prototype of the project.
CO4	Write the well-organized report with compiled results and comprehension with proficiency in English.
CO5	Develop the effective and innovative presentation using modern tools/software

M. Tech. II (VLSI & Embedded Systems) Semester – IV DISSERTATION PHASE - II ECVL202	Scheme	L	T	P	Credit
		0	0	40	20

1.	**Course Outcomes (COs):** At the end of the course, the students will be able to
CO1	Implement the proposed work with hardware /software resources and analyse results.
CO2	Compare the existing techniques and methods with proposed work.
CO3	Evaluate the results in terms of the performance parameters and further optimize the work for better solution.
CO4	Write the well-organized report with implemented results and comprehension with proficiency in English.
CO5	Attain the skills to solve real world problem in relevant area